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# AN AN/UYK-7 INTERPRETER IMPLEMENTED ON THE IBM SYSTEM/360

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# NAVAL POSTGRADUATE SCHOOL Monterey, California



AN AN/UYK-7 INTERPRETER IMPLEMENTED

ON THE IBM SYSTEM/360

bу

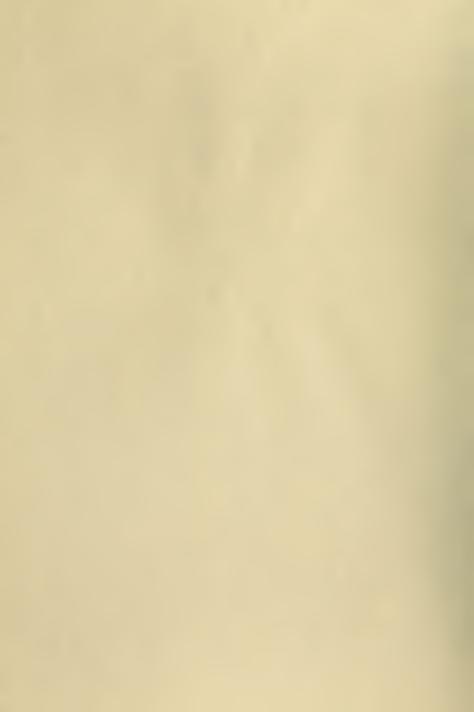
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December 1972

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An An-UYK/7 Interpreter Implemented on The IBM System/360

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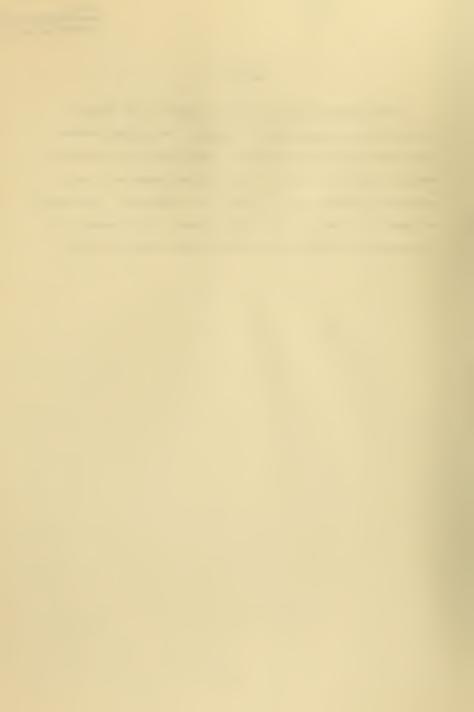
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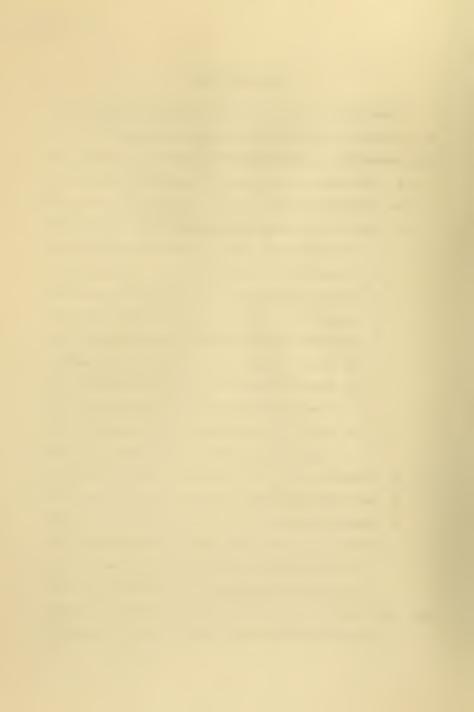
#### ABSTRACT

An IBM System/360 based interpreter program for the AN/UYK-7 multiprocessing computer system is presented. The program provides interpretive execution of the AN/UYK-7 instruction set, an interrupt-handling capability, a variable-sized simulated memory and a multi-processing capability for up to three central processors. Input/output is limited to a card reader and a line printer. Various segments of the program are discussed and a detailed User's Manual is provided.

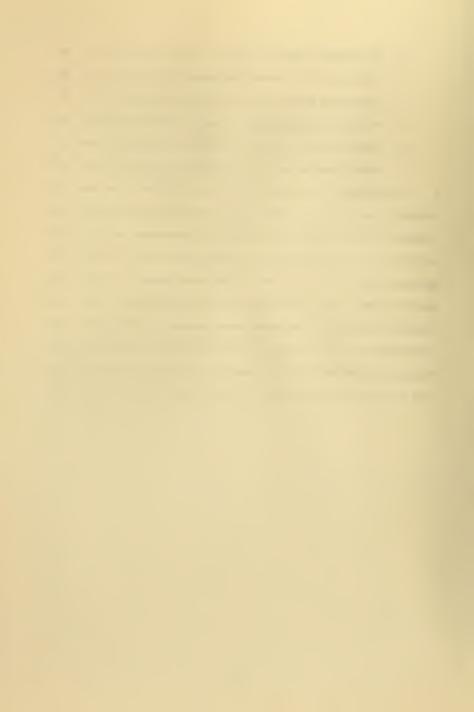


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#### I. INTRODUCTION

In the mid 1960's the U. S. Navy contracted with the Univac Division of the Sperry Rand Corporation for a reliable, ruggedized, multiple-processor computer system which would meet the stringent environmental and functional specifications for ship and shore requirements of the Navy. As a result, Univac produced the AN/UYK-7 which the U. S. Navy has purchased in quantity for NTDS shipboard applications.

Since many of the naval officers who will work with the AN/UYK-7 will be Computer Science graduates of the Naval Postgraduate School it was felt that some exposure to the AN/UYK-7 system would be beneficial. For lack of the hardware, an interpreter was desired as an educational aid.

The remainder of this thesis will not be concerned so much with how an actual AN/UYK-7 works as it will be concerned with how the interpreter has been implemented and how to use the interpreter as an educational aid. Some shortcomings of the implementation and areas which may be the subject of future research will also be presented.

The following sections are primarily designed as an explanation and guide for the user. It is assumed that the user is thoroughly familiar with [Refs. 1, 2]. For the casual reader who is more interested in a general overview, or not familiar with the AN/UYK-7, it is suggested that the detail in section III-C-5 and section IV (User's Manual) be bypassed.

Some of the particular features incorporated in the interpreter are:

- 1. Variable-sized simulated AN/UYK-7 memory;
- Multiprocessing;
- 3. Interrupt-handling capability.



The variable-sized simulated memory is covered in sections III-F (Memory and Paging) and IV-B (Job Control Language). Multiprocessing is covered in section III-B. Interrupt handling is covered in section III-D.

A minimum of 52K bytes of 360 memory is required to run any AN/UYK-7 configuration, however, with this minimum core, execution time may become unacceptable due to the paging demands.

#### II. DESCRIPTION OF THE AN/UYK-7

The AN/UYK-7 is a general-purpose, digital data computer with a multiprocessing capability that allows up to three central processors to operate simultaneously but independent of one another. Communication between the central processor (CP), memory units and I/O controller (IOC) is via a bused communication system consisting of three types of buses: instruction, operand and I/O. Each CP interfaces with the memory units via both instruction and operand data buses and with an IOC via an operand data bus. Every IOC communicates with the memory units via an I/O bus. Each CP is capable of addressing up to 16 memory units, a memory unit contains 16,384 words, 32 bits in length, and is capable of controlling up to four IOC's.

An IOC is capable of addressing up to 16 memory units and capable of communicating with external devices through an I/O adapter. The IOC can be controlled by a maximum of three different CP's. The I/O adapter is capable of communication with external devices via input and output channels that are provided in multiples of four. Each IOC has 4, 8, 12 or 16 I/O channels.



Each memory unit is capable of being addressed by any combination of CP's and IOC's, with the restriction that the total combined number of two accesses per CP and one access per IOC does not exceed eight memory accesses to any one memory unit.

Interface timing between computer units is handled on an asynchronous basis, wherein data transfers are performed via a request/acknowledge system. Each unit contains its own separate timing sources.

The computer contains three types of memory: main memory, control memory and non-destructive read out (NDRO) memory. Main memory is destructive read out memory consisting of three 16,384-word units.

Maximum expansion capability is 16 units (262,144 words). This memory stores all instructions and operands processed during normal programmed operation. The control memory consists of 82 flip-flop storage registers (CMR's) that hold up to 32 bits each. The control memory, located in the CP, stores data used for operand address modification, interrupt execution and monitor clock update operations. The NDRO consists of 512 hard-wired words.

The NDRO memory is contained in the CP and is a predetermined set of programs that are fabricated as a permanent part of the CP. The purpose of the NDRO memory is to provide a means of automatically loading control memory and main memory, provide a hardware fault analysis program and a load-failure analysis program.

Computer operations can be controlled from three different sources; the operator panel, the maintenance console and the remote console.

The operator panel initiates and controls normal on-line computer operation under program control. The optional maintenance console is used for off-line maintenance purposes. The optional remote console initiates



and monitors computer operations from a remote location. The maintenance and remote consoles are not required for system operation.

Execution of instructions by the CP is carried out in one of two modes, either the Interrupt or Task mode. The repertoire of the CP consists of 131 basic whole-word and half-word instructions of which 16 are priviledged instructions and are executable only in the Interrupt mode. There is a separate set of 27 instructions provided for the IOC.

The AN/UYK-7 accomplishes arithmetic in ones-complement form. Fixed point binary and floating point binary arithmetic are available. Fixed point arithmetic can manipulate either 32 or 64 bit operands. Floating point operands consist of two 32 bit fields which contain a sign extended 15 bit characteristic and a signed 32 bit mantissa.

### III. IMPLEMENTATION OF THE INTERPRETER

References 1 and 2 were the basic reference manuals used in the implementation. Disparities existed in both manuals concerning particular actions taken by the CP, and they were resolved by either background information or from outside sources. The outside sources were the Compiler Support Group and the SHARE-7 Group of the Fleet Combat Direction Systems Support Activity, San Diego, California.

#### A. PL360 LANGUAGE

PL360 is a language that provides all the facilities provided by System/360 Assembler Language yet exhibits an ALGOL-like syntax and control facilities. It was designed to improve the readability of programs written to take advantage of specific capabilities and limitations of the System/360.



PL360 was the language chosen over other suitable languages

(e.g., PL/1) primiarily because of the efficient code produced. Reference 3 contains a formal description of the language. The version used was the O/S - DOS version of December 14, 1971.

Since PL360 does not provide interface routines, a subroutine is contained in Appendix A which provides an I/O interface for a card reader, punch and line printer. Appendix B contains the subroutines necessary to accomplish page file management.

#### B. MULTIPROCESSOR LOOP

The Multiprocessor Loop (MPL) is entered after each instruction is completed or after the INTERRUPT procedure has completed its switching of registers. The MPL updates the IOC Monitor Clock and the Real-Time Clock. The IOC Monitor Clock interrupt is generated in the MPL. The IOC Monitor Clock and the Interprocessor interrupts are considered by the MPL and the active CP or designated CP respectively will process these interrupts. The MPL determines the CP to run next in a case statement using a variable for each CP called CPUSTATE to determine the status of the CP being considered. The possible CP states are:

- 1. Halted;
- 2. Wait (waiting for interrupt);
- 3. Interprocessor Interrupt;
- 4. Active;
- 5. IOC Monitor Clock interrupt generated.

Only functions that will generate states three or five will remove a CP from the wait state.

If a configuration with more than one CP is selected (section II-C) the CP's will execute one instruction each in a round-robin fashion beginning with CP zero. If a CP becomes inactive it will still be considered in the MPL but it will not execute instructions.



#### C. CENTRAL PROCESSOR AND BASIC INSTRUCTION SET

### 1. Central Processor

Each CP has 82 Control Memory Registers (CMR's) which contain all the accumulators, index and base registers for both states of the CP plus the necessary registers to perform storage protection. Because many of the registers in the CMR are of different length, all CMR's were implemented as full 32-bit registers (see Table 1). Two additional registers were added to the CMR's. They are hereafter referred to as SIMTIME and MAINSWITCH. SIMTIME contains the total execution time for the CP. For further details on timing see section III-G. MAINSWITCH was incorporated to allow the user to simulate the setting of various switches on the maintenance console which directly affect the results of an instruction. The switches are Jump 1, 2 and 3, Breakpoint, Stop 5, 6 and 7. To use them see section III-C. For initialization see section IV-E.

Each CP has its own set of CMR's and there is no communication or transfer of information between them. All CMR's are initialized to zero except the following:

- Active Status Register (ASR) is set in a Class IV interrupt state;
- 2. CP Monitor Clock has a value of negative zero.

To set the contents of the CMR prior to user program execution see .section IV-E.

Although the CMR's were implemented as 32-bit values, in very few cases may the user take advantage of this as the interpreter only uses those bits required by an instruction. Two points of the implementation are not explicitly explained in Ref. 1. The first being that ASR bits 10 and 11 determine which set of base registers, accumulators and index registers are used in processing an instruction,



not the state of the CP. For example, the CP is in Task state and bit 10 in the ASR is set and bit 11 is off. The instruction would use the Task set of base registers and the Interrupt set of accumulators and index registers. The second point concerns wrap around of the accumulators. If an instruction references accumulator A(a) and A(a+1) with the value of a being seven then accumulator A(a+1) is accumulator A(0).

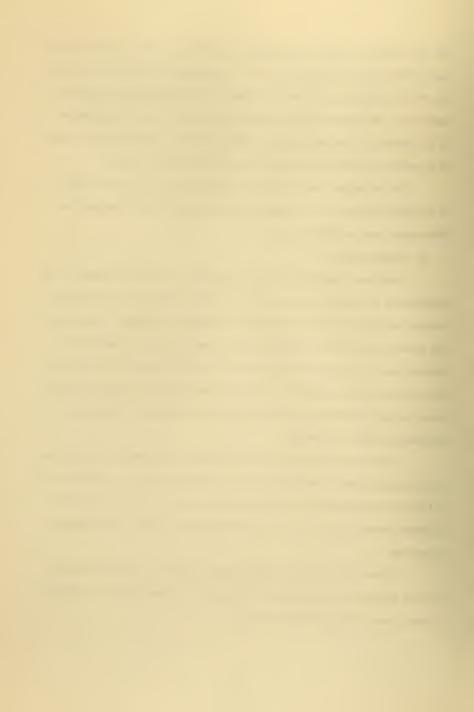
The Interrupt state has been defined as one of the bits 16-19 of the ASR being set. Bit seven of the ASR has no effect because the NDRO memory was not implemented.

# 2. Program Flow

Whole-word pre-processing is contained in the main program. The instruction is broken down into fields, indirect addressing is checked for and performed and the final operand address is computed. Based upon the function code, one of several procedures is called to perform the instruction. If abnormal termination or an error occurs in the instruction, the procedure INTERRUPT is called then control returns to the MPL. After normal completion, the TIME procedure is called to update the necessary clocks and SIMTIME.

For half-word instructions, the procedure HALFWORD is called and all pre-processing of the instruction is performed there. Normally, two half-word instructions are executed before control returns to the MPL. Abnormal termination of a half-word instruction invokes the INTERRUPT procedure.

If the lower half-word instruction, bits 15 - 0, is all zeros, then no operation is performed. If bits 31 - 26 are all zeros then an illegal instruction interrupt occurs.



## 3. Indirect Addressing

Indirect addressing is done prior to instruction execution in the pre-processing of the instruction. If character addressing is to be done the procedure MEMORY has the necessary information to obtain those bits requested when the operand fetch is done. When sequential character addressing is done the same information is available to the procedure MEMORY but the Indirect Address Word is modified as required and is stored back into the proper location prior to complete instruction execution.

A field modification to the AN/UYK-7 was performed concerning character addressing and is not contained in Ref. 1. For those particular instructions which use the k designator for quarter-word, half-word and whold-word operand reads or stores with character addressing specified in the Indirect Address Word, the k designator is ignored and the operand is processed according to specifications in the Indirect Address Word.

If an instruction specifies character addressing and it is not allowed, a CP Illegal Instruction Error interrupt occurs.

# 4. Repeat Mode

The normal flow in the interpreter is the processing of one instruction then control returns to the MPL. The "Repeat" instruction (RI), function code 076, alters this flow. Upon execution of the RI, control returns to the whole-word pre-processing section. If the next instruction is not repeatable then a CP Illegal Instruction Error interrupt is generated.

For termination in the non-compare instructions with the k designator in the RI being either five or six the contents of A(a) in the repeatable instruction are checked for even or odd parity.



A field modification to the AN/UYK-7 not contained in Ref. 1 concerns character addressing when it is specified in the repeatable instruction. The instruction is performed one time and B(7) is set to zero. If sequential character addressing is specified, the Indirect Address Word is modified appropriately, stored away and the instruction is done one time with B(7) set to zero.

# 5. Instruction Format Description

The central processor instruction set is divided into five typesFormat I, II, III, IVA and IVB. Format I, II and III are whole-word
instruction, 32 bits in length. Format IVA and Format IVB are half-word
instructions, each 16 bits in length. See Refs. 1 or 2 for field designators and details of the instructions.

### a. Format I Instructions

Format I instructions cover function codes (hereafter referred to as opcodes) 10 through 47 and 54 through 57. Opcodes 10 through 47 utilize the k) designator to specify whether the operand is read from or stored into memory in whole-word, half-word or quarter-word form. When the k designator is interpreted as a normal read instruction (memory to arithmetic), the procedure NORMREAD performs this function. The procedure NORMSTORE handles the case when the k designator is interpreted as a normal store instruction (arithmetic to memory). If the k designator is interpreted as a normal replace instruction the procedure NORMREAD is used for the read portion and the procedure NORMSTORE is used for the store portion.

For the normal store and normal replace instructions with the k designator equal to zero, a no operation instruction occurs. If character addressing is done (see section II-C-3) the k designator is ignored and character addressing is performed as required by the instruction.



For example, opcode 24 stores A(a) into the memory cell specified by the computer operand address. For k not equal to zero and no character add addressing, one of seven cases of NORMSTORE will be done; with k equal to zero and no character addressing, a no operation instruction is performed. If character addressing is specified, the accumulator is stored according to the specification of the character addressing, regardless of whether k is zero or not.

Opcodes 11 and 25 with the b designator equal to zero or opcodes 20 through 23 and 43 with the a designator equal to zero are executed as no-operation instructions. Opcodes 31, 32 and 42 are not replace instructions even though a disparity exists in Ref. 1 concerning this point. If the ak value is greater than 40, a no-operation instruction is done.

Opcodes 54 through 57 do not use the NORMREAD or NORMSTORE procedures. The k designator is special and is used as specified. As explained earlier, all CMR's are implemented as 32-bit fields. When executing opcodes 54 and 55, all 32 bits of the contents of Y are loaded execpt when CMR address 6X is used. The lower 15 bits are loaded and the upper bits are not affected. Opcode 56 and 57 store the full 32 bits into Y. For all four instructions, if CMR addresses 30 through 57 or 130 through 137 are accessed, a CP Illegal Instruction Error interrupt is generated. When a CMR is accessible in the Interrupt mode only, i.e., addresses 20 through 177, and the CP is in the Task mode, a Privileged Instruction Error interrupt is generated. For the rest of the Format I instructions no restrictions are placed upon the user except as noted in Ref. 1.



#### b. Format II Instructions

All fields are used in accordance with Ref. 1.

Opcode 06, with f2 equal to zero, one, two or three, is implemented utilizing bit manipulations and integer arithmetic due to the fact the 360 floating point hardware will not handle values acceptable in the AN/UYK-7. The same restrictions as they apply in Ref. 1, are required in the use of these opcodes.

Opcode 06, with f2 equal to four, five, six or seven, is not implemented and will return the same results as the corresponding opcode 06 instruction with no round.

Opcode 07, with f2 equal to one, two three or four ignores the designator because only one IOC was implemented. Opcode 07, with f2 equal to four, invokes the IOC procedure. In opcode 07, with f2 equal to five, the lower 20 bits of the Active Status Register (ASR) are replaced. This is the only place where bits 16 - 19 of the ASR may be changed by software other than in the INITIALIZE procedure. In other words, by altering the appropriate Designator Storage Word in the CMR, an ASR may be built to the user requirements. See section III-C-4 for an explanation of opcode 07 with f2 equal to six.

#### c. Format III Instructions

For all opcodes, the k designator, bit 20, must be zero. If not, a CP Illegal Instruction Error interrupt is generated. In opcode 53, with f3 equal to two or three and the a designator greater than zero, a variable called MAINSWITCH is accessed to see if the switch is set (see section II-C-1). These switches are set during the initialization phase (see section IV-E) and can not be altered once execution has begun. If the stop switches are selected and are on, the particular CP executing that instruction halts and can not be restarted.



#### d. Format IVA Instructions

In opcodes 60 and 61, 32 bits are transferred except for the following CMR addresses:

- 1. For CMR 11 through 17 and 111 through 117, only the lower 16 bits are moved;
- 2. For CMR 7X, in opcode 61, only the lower 15 bits are moved, the upper bits remain the same.

Opcode 74, with f4 equal to two, was implemented by a binary search and first approximation method since available square root routines would not handle a 64-bit integer. For opcode 74, f4 equal to three and the b designator equal to zero, the index register specified by the a designator is zeroed out. In opcode 74, f4 equal to seven, two special cases occurred. If the b designator is zero then B(a) is compared with zero, and/or if the a designator is zero then B(b) is compared with zero. The a designator in opcode 77, f4 equal to zero or one, is ignored since there is only one IOC. For opcode 77, f4 equal to six and the i designator is zero, the CP executing this instruction halts and can not be restarted. With the f4 designator equal to one, the only interrupts that will change the state of the CP are in Interprocessor interrupt or an IOC Monitor Clock interrupt, provided this particular CP receives the IOC Monitor Clock interrupt.

#### e. Format IVB Instructions

The procedure SHIFTAMT, interprets the m designator and performs the proper shift. If the shift amount is contained in B(b) and the b designator is zero, a no operation instruction occurs.

#### D. INTERRUPTS

The INTERRUPT procedure is implemented to set up the CP for all interrupts of Class II, III, IV and limited Class I interrupts (addressing



locations outside of the physical memory of the AN/UYK-7). Since
the NDRO is not implemented, all interrupts load the branch address from
the appropriate Initial Condition Word into the P register. Interrupts
are generated when detected and INTERRUPT is called immediately with
register one containing the class and register two containing the Interrupt
Status Code. Interrupts are not queued due to the serial nature of the
interpreter. The CP presently active (last executing) will process the
interrupt generated with the exeception of the two interrupts considered
in the MPL.

In INTERRUPT the p register and the old Active Status Register (ASR) are stored in the control memory of the CP and the ASR is changed as appropriate for the class of interrupt (Ref. 1 or Ref. 2).

## E. INPUT-OUTPUT CONTROLLER

The IOC was implemented to closely simulate the actual IOC even though in a few instances reductions could have been made in the coding at the expense of realism. When the CP calls the IOC to do an instruction or a series of instructions (chaining) the IOC maintains control until it completes its instructions or an interrupt is generated in the IOC. This implementation of completing a series of IOC instructions before control is returned to a CP prevents the use of (or the requirement for using) a'Wait for Interrupt' instruction by the CP to ensure the buffer area is filled or emptied before processing can continue. When an interrupt is generated, control is returned through INTERRUPT to the MPL to process the interrupt and any instructions remaining in the IOC chain are not executed. This is one main difference from the actual AN/UYK-7 IOC.

Buffer instructions are terminated by filling or emptying the buffer since the 'Terminate' instruction could not be efficiently implemented. Other



instructions not included in the IOC are the 'External Interrupt' and 'External Function' instructions since devices were not available to simulate these types of data transfers. The k designator in the IOC instruction field is implemented only to indicate data suppression or data transfer and not half-word or byte transfers as in the AN/UYK-7 (Refs. 1 and 2).

Two channels have been included in the IOC. Channel five is the card reader and channel six is the line printer. Input and output to these devices will be in EBCDIC format to run on the IBM-360. Capability to include other I/O devices on other channels requires modifying the case statement for each channel number.

### F. MEMORY AND PAGING

The memory of the AN/UYK-7 is simulated in multiples of 1024 word modules or pages. An actual AN/UYK-7 would have some multiple of 16,384 words of memory, each word containing 32 bits. However, 16,384 words of AN/UYK-7 memory are the equivalent of 65,536 bytes of 360 memory. In order to reduce memory requirements, the interpreter program allows memory requirements to be defined in multiples of 1024 words or 4096 bytes. A user supplied control card defines the number of pages the job will require. Whether or not paging will be required is then determined internally by the program. By performing a shift left of 12 bits on the number of modules requested, the program determines the number of bytes required for the AN/UYK-7 memory. If the region declared for the GO step is adequate to allow the requested number of bytes to be obtained through the execution of a variable GETMAIN macro then the AN/UYK-7 memory will be wholly contained in core within the program. A logical flag called PAGING will remain false.



If the number of pages of AN/UYK-7 memory exceeds the region obtained by the GETMAIN macro then PAGING is flagged as true and the page file is created on disk. This occurs within procedure INITIALIZE. The page file is created as a Basic Direct Access file. When paging will be required, the user should ensure that the GO.PAGEFILE JCL card (see section IV-B) specifies at least as many records as the number of pages requested or the program will terminate during file initialization due to lack of file space on disk.

Procedure MEMORY contains the programming which performs all AN/UYK-7 memory references. MEMORY contains internal procedures FETCHPAGE,

MEMINTERRUPT, MEMFETCH and MEMSTORE. MEMFETCH performs all AN/UYK-7 memory fetch references while MEMSTORE performs all AN/UYK-7 memory store references. When paging is in effect, either MEMFETCH or MEMSTORE may call FETCHPAGE due to a virtual page not being core resident. MEMINTERRUPT is called either by MEMFETCH or MEMSTORE whenever a requested AN/UYK-7 memory reference is outside of the defined limits of memory as described by the control card statement. MEMINTERRUPT then sets up the parameters and calls procedure INTERRUPT. All Class I interrupts that can be handled in software are generated in this manner.

Procedure FETCHPAGE contains the page replacement algorithm. The array PAGETABLE is scanned to a depth equal to the number of virtual pages if necessary, searching for a page which is described by one of the four cases which follow:

- 1. In memory, unchanged, not recently referenced;
- 2. In memory, unchanged, recently referenced;
- 3. In memory, changed, not recently referenced;
- 4. In memory, changed, recently referenced.



Given the worst situation case four will occur. If case one or two occurs then the page need not be written out. If case three or four occurs then the page must be written out and then replaced by the new page.

The foregoing cases are encoded in a status byte in the high-order byte of each virtual page entry in PAGETABLE. The eight bits (7-0) of the status byte are used in the following manner. Bit seven, the high-order bit, is on if the virtual page is core resident and off if not core resident. Bit six is on if the page has not had a store reference, otherwise bit six is off to indicate that the page has been modified. Bit five is on if the page has not been referenced since the last page fetch occured. This is due to the fact that all pages are changed to indicate an unreferenced condition when a new page is loaded into memory by PAGEFETCH.

The remaining bits (4-0) of the status byte are unused.

Within each virutal page entry in PAGETABLE, the lower-order byte contains the physical page number (relative block address in memory) that the virtual page occupies or last occupied. When a virtual page is replaced, its physical page number is placed in the lower-order byte entry of the replacing page. Thus the physical page numbers are passed from virtual page to virtual page.

When paging is not required, the AN/UYK-7 address together with the starting address of the AN/UYK-7 memory area in core are used to directly compute the 360 address.

All calls to MEMORY pass a value in register one. The value in register one determines which type of memory request is being made via execution of a case statement. The first three cases are instruction fetch, operand fetch and operand store. For the operand store case, the value to be stored is assumed to be in register two. Each case carries out the appropriate storage protection checks if required. Cases four



and five are unconditional memory fetch and store cases used by the IOC since the IOC is not in any way restricted by storage protection. Case six is also an unconditional fetch case. This is due to normal store instructions which insert bytes into a word in AN/UYK-7 memory without fetching the word. Since MEMORY only fetches and stores whole-words a fetch must be made initially for the word in question in order to construct the final word. If the fetch were to violate storage protection in some way then an interrupt would be generated for a fetch violation by an instruction which supposedly does not fetch. Thus case six bypasses the problem since the following store operation will cause the proper interrupt if the storage protection conditions are appropriate. Case seven handles indirect addressing references. After storage protection checks for the indirect case are completed the program loops back to the case for operand fetching to complete the remaining storage protection checks.

If any call to MEMORY succeeds in passing the checks of the appropriate case or cases then ultimately a call will be made either to MEMFETCH or MEMSTORE. It is noteworthy that initialization and dump of AN/UYK-7 memory call MEMORY using cases four and five.

#### G. TIMING

# 1. AN/UYK-7 Clocks

All clocks indicate time in tenths of microseconds. The CP Monitor Clock initially set negative is updated after the completion of each instruction by the time required for the AN/UYK-7 to execute the instruction. SIMTIME is incremented by the same amount. The IOC Monitor Clock, initially set negative, and the Real-Time Clock, initially set zero, are updated in the MPL by an average time of two microseconds.



# 2. Speed Of The Interpreter

The sample program (see Computer Output) ran on the IBM-360

Model 67 with an average execution time ratio of 360 to 1. When memory
and register dumps and trace were eliminated the sample program executed
with a ratio of 240 to 1. It is noteworthy that the IOC time of the

AN/UYK-7 is not included in SIMTIME from which these ratios were calculated.
This implementation would provide accurate timing only if there was 100%
overlap between CP execution and I/O and there was no interference between
the CP's and the IOC.



# IV. USER'S MANUAL

To utilize the interpreter the user must be familiar with the AN/UYK-7 instruction set and format and have a general understanding of the system configuration and requirements. The procedures INITIALIZE and INITIALIZ2 build a system for the user from data on control cards, allow presetting of the CMR's from data cards and allow loading of instructions and data into memory from instruction and data cards. The procedure INITIALIZE has very few error messages, therefore, when a field on the inputed card is either alphabetic or numeric, the user must assure that it follows the specification or a 360 system error may result.

# A. INITIAL PROGRAM LOAD

CMR's 00 through 6X, 100 through 107, 111 through 177 and the Real-Time Clock have been initialized to zero. CMR 6X (ASR) has been initialized to a State IV interrupt condition. The CP Monitor Clock (CMR110) and the IOC Monitor Clock are initialized to negative values. The initialization of the CMR's applies to all three CP's. MAINSWITCH, the variable representing the switches on the maintenance console for each CP is initialized to zero. This means the Jump 1 - 3 and Stop 5 - 7 switches are off and the Breakpoint switch is set to the Program mode. SIMTIME is initialized to zero.

The zeroing of the CMR's has several important implications. First of all, since all of the Initial Condition Words for all of the CP's are preset to zero, all interrupts for any CP will cause instruction execution to branch to location zero in memory. Secondly, the Breakpoint CMR value



will not be checked because bits 18 and 19 will be off. Thirdly, initial execution in the Task state will immediately result in an interrupt because the storage protection registers are zeroed. Thus the user must insure that all applicable CMR's are properly set.

The CP Monitor Clock and the IOC Monitor Clock are set to negative values in order that the first instruction executed by a CP does not create an interrupt.

#### B. JOB CONTROL LANGUAGE

In Appendix C, there are two sets of Job Control Language (JCL) to cover the needs of the user. The reference to the AN/UYK-7 program in the JCL refers to data loaded into the interpreter and the PL360 program refers to the code for the interpreter.

If the user does not desire to build a load module on disk, the SYSLMOD card should be modified accordingly. In the first set of JCL there are two parameters which may be varied depending upon the size of AN/UYK-7 memory desired. They are the region parameter on the GO EXEC card and the space parameter on the GO.PAGEFILE card. See the next section for amplication.

# C. CONTROL CARDS

There are six control cards and each one must be supplied or the program will terminate with an appropriate message. It should be stressed again that the formats for the cards be exactly followed or a 360 system error may result.

The first card specifies the number of 1K (words) segments of AN/UYK-7 memory. The number must be numeric and right-justified in columns one through three. If a value greater than 256 is requested, only 256 segments



will be allocated. The range of AN/UYK-7 memory address will be from zero to 1024 times the number of pages specified by the control card less one.

The interpreter and system routines require approximately 48K bytes of 360 core. The GO.PAGEFILE card will be required if not enough core is specified to contain the requested number of 1K segments (pages) of AN/UYK-7 memory. An easy method of determining whether the GO.PAGEFILE card is required is to take the region parameter specified on the GO EXEC card minus 48K and divide the result by 4K. The answer will be equal to the number of pages in core and if the number of pages requested exceeds the number in core the GO.PAGEFILE card is required with the space parameter as SPACE = (4096, number requested on control card).

Example 1: The user has allocated 100K for the GO step (i.e., REGION = 100K) and on the control card requests 13 segments of AN/UYK-7 memory. By the formula, (100K - 48K)/4K = 13, no paging is required. Therefore, the GO.PAGEFILE card is not required.

Example 2: The user has allocated 100K for the GO step and requests on the control card 20K (words) of AN/UYK-7 memory. Again, by the formula, the number of pages would be 13 and would be less than the number of pages requested in the control card. Therefore, paging will be required and the GO.PAGEFILE must have the space parameter specified as SPACE = (4096,20) or a 360 system error will occur.

The second control card specifies the number of CP's wanted. The number must be numeric and in column three. If the value is zero or greater than three, a message will be printed and the program terminated. CP numbers are allocated beginning with zero. Upon program execution those CP's allocated will be in an active state and will commence executing instructions.



The third control card specifies the sections of memory to be dumped at normal program termination. At least one and up to six different sections can be dumped. The card format is as follows:

- 1. Column 1 and 2 "MD";
- 2. Columns 4-9, 17-22, 30-35, 43-48, 56-61 and 69-74 contain a six digit decimal number for the lower bound addresses;
- 3. Columns 10 15, 23 28, 36 41, 49 54, 62 67 and 75 80 contain a six digit decimal number for the upper bound addresses.

If any of the following conditions occur, that field and the remainder of the card are ignored:

- Column 9, 15, 22, 28, 35, 41, 48, 54, 61, 67, 74 or 80 is blank;
- The lower bound address is greater than the maximum memory address;
- 3. The upper bound address is greater than the maximum memory address;
- 4. The lower bound address is greater than the upper bound address.

The fourth card specifies which Control Memory Registers (CMR's) are to be dumped at normal program termination plus options concerning instruction input. There are 177 (octal) CMR's plus the P register, SIMTIME and MAINSWITCH or 202 (octal) registers. Any one consecutive section of the 202 registers may be dumped. The format of the card is as follows:

- 1. Columns 1 and 2 have "RD";
- Columns four through six contain the lower octal CMR address (must be zero or greater);
- 3. Columns eight through ten contain the upper CMR address (must be zero or greater and less than 203).

If the upper address is less than the lower address a partial dump will occur. The two fields must be octal values, right justified in the proper columns with no blanks and supplied.

The next three fields on the register dump card concern the instruction input. In columns 12 and 13 a "PI" will print the cards with octal instruction format along with their load address. If "PL" is put in columns 15 and 16 then the data values inputed are echo-printed out.

Columns 18 and 19 specify which instruction input is to be used. "F1" is



used for octal instruction format and "F2" is used for object instruction format. The defaults for the three fields are no instruction print, no data print and octal instruction format.

The fifth card allows the user to trace instructions in execution.

The trace is printed when the address for the instruction falls within the trace card limits. Instructions executed by the 'Execute Remote' instructions are not traced.

This card is scanned based upon the number of CP's specified, i.e., if three CP's are requested then three fields (for CP zero, CP one and CP two in order) are scanned. The format of the card is as follows:

- Column 1 contains a "T";
- 2. Column 2 contains a blank or "N", if "N" then no trace is provided;
- 3. Columns 3 8, 17 22 and 31 36 are a six digit decimal address for the lower bound on the trace;
- 4. Columns 10 15, 24 29 and 38 43 are a six digit decimal address for the upper bound on the trace.

If a trace is not wanted for a particular CP with two or three CP's requested then the upper bound address must be less than the lower address.

On the memory dump, register dump and trace control cards, all numbers must be right justified in their respective columns and contain no alphabetic characters. The only numeric fields which are not decimal are two fields on the register dump card. The last card has a "%" in column one to signify the end of the control cards.

#### D. INSTRUCTION INPUT

The two formats for inputing instructions are octal and object. The octal format closely represents the AN/UYK-7 format for instructions and the object format is a binary output from an assembler or compiler.

The octal format has eight fields for whole-word instructions and follows the format of Format I instructions. Columns one through five



on the card contain the first five octal numbers of the instruction and column six has a zero or one to indicate the indirect address designator off or on respectively. Column seven contains the octal base register number and columns eight through eleven contain a decimal number less than 8192 for the basic operand address. For example, if the number 53423161238 was contained on the card in columns one through eleven it would be interpreted as function code 53, a designator equal to four, f3 designator equal to one, k designator of zero, b designator equal to three, i designator on, s designator of six and a basic operand address of 1238.

Half-word instructions have 12 fields and follow the format of Format IVA instructions. Fields one through five and seven through eleven are the first five octal fields, respectively, of two half-word instructions. Fields six and twelve are a zero or one bit for the i designator. If the half-word instruction is a Format IVB instruction the m designator is in fields four through six or fields ten through twelve. An example of two half-word instructions is 716230627450 and it would be placed in columns one through twelve. The interpretation of the upper half-word would be a function code 71, a designator equal to six, an f4 designator of two, the designator equal to three and the i designator off. For the lower half-word, the instruction would be interpreted as function code 62, the a designator equal to seven and the m designator equal to 450 which means the shift amount is in B(5).

Instructions are loaded sequentially beginning at memory address zero unless a decimal address is specified in columns 15 - 20 of the card. If an address is specified then the instructions are loaded sequentially from that address. Consecutive instructions do not require an address field. Any time an address exceeds the maximum address available in memory and error message is printed and execution is terminated.



Columns 21 - 80 are available for comments. Only the three low-order bits are inspected when an octal field is specified and for binary fields, the low-order bit is inspected. The two decimal fields on the card are the basic operand address and the load address and must contain only decimal digits or a 360 system error will occur. See the Computer Output for examples of octal instructions.

The object format does not perform any card conversion as all eight bits of a single column are used. The first three columns represent an 18-bit address where the first instruction on the card is to be loaded into memory. The next column contains the number of four character fields to be placed into memory. A number of 1 through 19 is required and the value is used to scan the card. Columns 4 - 80 contain 19 four character fields in which all 32 bits are loaded into memory.

The last card for the object format inputs the P register values for the number of CP's specified by the CP control card. A "P" must be placed in column 4. Columns 5 - 8 are for the P register value for CP zero, columns 9 - 12 are for the P register value for CP one and columns 13 - 16 are for the P register value for CP two. Only the lower 20 bits are used of the 32 bits inputed.

The "PI" option explained earlier echo-prints the octal format and not the object format. The last card after either the octal format instructions or the object format instructions is a card with "%" in column one.

#### E. DATA AND REGISTER INPUT

To allow the user complete flexibility in specifying the initial state of the AN/UYK-7, the ability to input values into memory or override the



initialized values of the registers, i.e., the 177 CMR's, P register, SIMTIME and MAINSWITCH, was incorporated.

To load data into memory the card format is as follows:

- 1. "D" in column one;
- 2. A six digit decimal number less than the maximum memory address
- in columns three through eight;
- 3. The hexidecimal value to be loaded in columns 10 17.

To load the registers the card format is as follows:

- 1. "R" in column one;
- 2. A six digit decimal number from Table 1 in columns three through eight;
- 3. The hexidecimal value to be loaded in columns 10 17.

To load the registers for CP one, add 85 to the number obtained from Table 1 and for CP two, add 170 to the number obtained from Table 1.

MAINSWITCH is comprised of seven switches as follows:

- 1. Jump 1 in card column 10;
- 2. Jump 2 in card column 11;
- 3. Jump 3 in card column 12;
- 4. Breakpoint in card column 13;
- 5. Stop 5 in card column 14;
- 6. Stop 6 in card column 15;
- 7. Stop 7 in card column 16.

To turn on a switch or to set Breakpoint to Manual mode, a "1" is punched in the indicated column. A zero sets the switch off or the Breakpoint to Program mode. For example, 01010000 will set the Jump 2 switch on and the Break point to Manual mode.

When the ASR is loaded only the lower 20 bits are placed in that register to preserve the CP number.

## F. SPECIAL NOTES

After a proper initialization sequence the CP and memory configuration is printed out. Then the message, "START EXECUTION," is printed and execution of the AN/UYK-7 instructions begin. The message, "END EXECUTION," is printed if and only if normal termination of the program occurs.



It is strongly advisable to load a 'Halt' or 'Wait' instruction at location zero or provide an interrupt handler for unexpected AN/UYK-7 interrupts. An OC7 System/360 error may occur as a result of improper data, instruction or control cards.

### G. EXAMPLE PROGRAM

The computer output contains an example of an AN/UYK-7 program executed by the interpreter. Following the header line, "OCTAL INSTRUCTION FORMAT," is a program listing which is an echo-print of the instruction cards preceded by their decimal load points.

In the example program, CPO executes the code between and including locations 100 and 155 while CP1 executes the code between and including locations 1030 and 1080.

CPO has the task of reading in data cards, echo-printing the input, converting the EBCDIC code to a somewhat modified unpacked decimal format and storing the result in an array starting at location 2100. When a number is stored in the array, location 2048 receives the updated address pointing to the last location in the array. When CPO reads a blank card signifying end of data, a flag at location 2049 is set to zero. CPO then executes a 'Wait for Interrupt' instruction. In the meantime, CP1 starts testing location 2048 to determine if there are at least two values in the array. As soon as there are two values in the array, CP1 begins a modified ripple sort. Each time, prior to fetching a number from a deeper position in the array has not been reached. If the deepest position in the array has been reached then location 2049 is tested in order to determine whether or not the array is complete.



When the sorting has been completed, CP1 enters the Interrupt state, sends an Interprocessor interrupt to CPO and then halts. This action restarts CPO which then reconstructs the number into EBCDIC format (with leading zeros suppressed), prints out the array and then halts.

As may be seen from the output, a list of the input data follows the "START EXECUTION" header line. The result of the program may be seen following the example trace of instructions.



## V CONCLUSIONS

The benificial aspects of the interpreter as an educational aid for the student are twofold. First, the interpreter may be used as an educational aid to demonstrate and teach the principles involved in building operating systems and interrupt handlers. The principles of multiprocessing and multiprogramming may be taught by utilizing software without the requirement for the necessary hardware. At the present time, the Naval Postgraduate School does not have readily available a suitable software teaching aid for operating system principles. The AN/UYK-7 interpreter, possibly modified to run under a time-sharing system, would provide this capability. Secondly, the interpreter will give the student the ability to investigate and evaluate problem areas of the Navy's command and control systems. It will also provide a means of familiarization with the AN/UYK-7 for future "Fleet" users.

To the researcher, the interpreter is a tool for evaluating or improving existing operating systems for the AN/UYK-7. New concepts for subsystems for the Navy's command and control systems may now be devised and tested without the previously necessary hardware.

A brief review of present day interpreters reveals three important facts. First of all, most interpreters do not provide I/O on the simulated computer, and second, available memory in the simulated computer is often restricted. Finally, multiprocessing generally cannot be performed in a manner adquate to test and evaluate multiprocessing systems. The AN/UYK-7 interpreter provides limited I/O capability. However, this limitation may be overcome by incorporation of external I/O routines or implementation of additional IOC channels (see Appendix D for amplification).



The variable AN/UYK-7 memory realized in the interpreter allows the user a spectrum of options. These options vary from a minimum core requirement of 52K bytes, with the associated paging overhead, to maximum available core, with reduced or eliminated paging overhead.

The use of the PL360 language versus several other production type higher-level languages has afforded the user a reduced execution time per AN/UYK-7 instruction. The execution speed ratio is considerably lower than that in many other interpreters.

Due to insufficient time and the various permutations and combinations of instructions and data, it was not possible to completely test all instructions.

Areas of future study for using or improving the AN/UYK-7 interpreter are listed as follows:

- 1. Implemention of an operating system including a "Bootstrap" for the interpreter;
- Investigation of operating systems for "Fleet" use on the AN/UYK-7;
- 3. Implementation under a time-sharing system (with the ability to display/modify registers and memory and restart the program);
- 4. Investigation of application programs limited only by the I/O devices available:
- 5. Implementation of additional IOC channels to provide better I/O capabilities;
- 6. Implementation of an assembler for use with the interpreter.



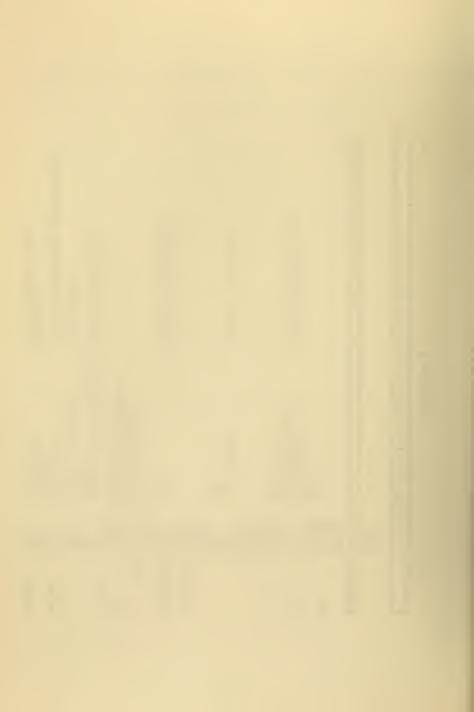
### CONTROL MEMORY ADDRESS TABLE

	CMR	ADDRESS	DESCRIPTION OF					
(OCTAI	(۱)	(DECIMAL)	ECIMAL) CONTROL MEMORY ADDRESS					
			r					
0 -	7	0 - 7	TASK ACCUMULATORS	32 EA				
	10	8	UNASSIGNED (ADDRESSABLE)	19				
11 -	17	9 - 15	TASK INDEX REGISTERS	20 EA				
30 -	57		UNASSIGNED (NOT USABLE)					
60 -	67	24	BREAKPOINT REGISTER	20				
70 -	77	25	ACTIVE STATUS REGISTER	23				
100 -	107	26 - 33	INTERRUPT ACCUMULATORS	32 EA				
	110	34	CP MONITOR CLOCK	19				
111 -	117	35 - 41	INTERRUPT INDEX REGISTERS	20 EA				
120 -	127	42 - 49	INTERRUPT BASE REGISTERS	18 EA				
130 -	137		UNASSIGNED (NOT USABLE)					
140 -	157	50 - 65	DSW AND ICW REGISTERS	20 EA				
160 -	167	66 - 73	STORAGE PROTECTION REGISTERS	21 EA				
170 -	177	72 - 81	STORAGE IDENTIFICATION REGS	21 EA				
	200	82	P REGISTER	20				
	201	83	SIMTIME	32				
	202	84	MAINSWITCH	32				

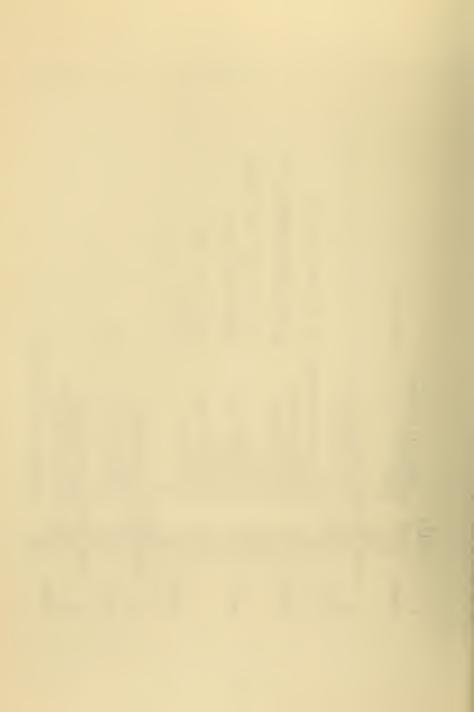
Table 1



	474	ICTL 1.71。8PAC # 1.71。18		SAVE REGISTERS ESTABLISH ADDRESSING	RESTORE REGISTERS	PRINTER LINE LENGTH		TEST FOR OPEN DCB	TEST FOR PREVIOUS END-OF-FILE	GET CARD SET CONDITION CODE
ALI ENOTA		TL 1.71.18 AACE **********************************	CACE TARA TARA ATTER ATT	STM 12, 2, 5 SAV E 12, 12, 5 SAV E 12, 12, 12, 12, 12, 12, 12, 12, 12, 12,	17 12,2,SAVE 14 14 15 16 17 18 18 18 18 18 18 18 18 18 18 18 18 18	ACCT C C I 3 2 NO 3 E N	ACE PROCEDURE READ(R14) 0) = BUFFER ADDRESS 13) = SAVE AREA ADDRESS 14) = RETURN ADDRESS	SYSIN+DOPEN,OPENMASK READI 2,00 (SYSIN,(INPUT))	1 EOF+X*FF*	T SYSIN•(0)
	************	I C J S S S S S S S S S S S S S S S S S S	S E P	SEP NO DESCRIPTION OF SEPTIMENT	MJ@UEV	SPL360IO CSP LINELEN EQU LINESMAX EQU	GLOBAL F	2	READ1 CLI	READ2 CLI



```
R
                                                                                                                                                                                                                                                                            ESET LINE COUNT AND SPACING
                                                                                                                                                                                                                          GET NEXT BUFFER ADDRESS IN SUPPLY CONTROL CHARACTER
                                                                                                                                                                          2.00
WRITE1
(SYSOUT+DOPEN,OPENMASK TEST FOR OPEN DATA SET
(SYSOUT)
(OI) 1),CARCONT
(CARCONT,C.1)
                                                                EODAD EXIT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       SET
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      SYSPUNCH+DOPEN,OPENMASK
PUNCH1
*PEOD EXIT ROUTINE
EOF, X FF;
READ2
                                                                                                                                                                                                                                                                                                                                                                MYI CAREGOTT.C.1.
LM CAREGOTT.C.1.
LM CAREGOTT.C.1.
LM CAREGOTT.C.1.
SPACE 2
SAL PROCEDURE PAGE (R14)
ENTRY PAGE
WITHY PAGE
OSTROCONT.C.1.
BR 14
SPACE 2
CARCONT.C.1.
SR 14
SPACE 2
BUFFER ADDRESS
(R14) = SAVE AREA ADDRESS
(R14) = RETURN ADDRESS
ENTER SYSPUNCH+DOPEN,GPEN
                                                                                      EXIT
SPACE
                                                     USING
MVI
B
                                                                                                                  GLOBA
                                                                                                                                                                                                                                                                                                                                                                                                                                       GLOBA
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           GLOBA
                                                                 ENDROR
                                                                                                                                                                                                                                                                                                    WRITE2
                                                                                                                                                                                                                                                                                                                                                                                        WRI TE3
                                                                                                                                                                                                                             WR I TE 1
                                                                                                                                                                WRITE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           PUNCH
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       PAGE
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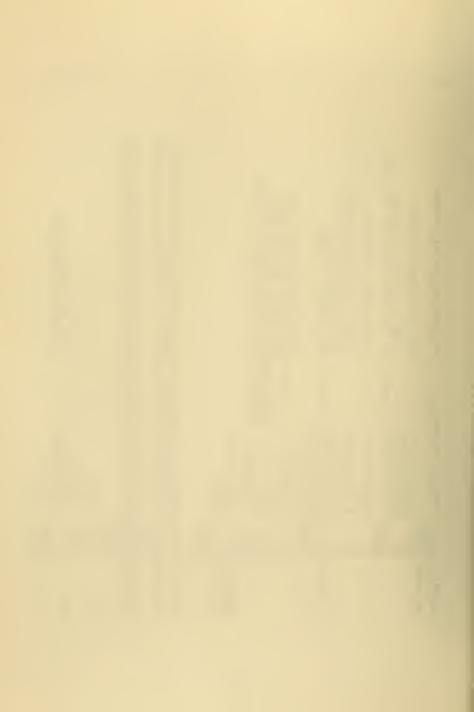
		×	×	×				
TPUT ) )	PUT CARD IMAGE	F=PL,DDNAME=SYSPRINT,DEVD=DA,RECFM=FBA,+1,BFTFK=S,FRDPT=ABE	F=6M.DDNAME=SYSIN,DEVD=DA,RECFM=FB,	DSSR G=PS, MACRY=PY, NONAME=SYSPUNCH, DEVD=DA, RECFM=FB,		PRINTER LINE COUNT PRINTER CARRIAGE CONTROL	CB BYTE SET BY OPEN	
(SYSPUNCH, (OUTPUT))	ŠÝŠ PUNCH, (O)	DSORG=PS • MACRI	DSORG=PS MACRI	DSDRG=PS,MACRI	7F	100- 100- 0XX	DCBOFLGS-IHADCB X'10'	
LR OPEN		DCB DCB	DCB	DCB	SOC	000 000 000 000 000 000	CSECT EQU EQU	END
	PUNCH1	SYSOUT	SYSIN	SYSPUNCH	SAVE	LINECNT CARRCONT	\$PL360I0 DOPEN OPENMASK	



PROCEDURE 3ETFRAME	SPACE MACRO ENTRY & EPP 15 ENTRY & EPP 15 USING 12,2,5AVE SAVE REGISTERS STM 12,2,5AVE ESTABLISH ADDRESSING	SCSECT SETC SETCE SETCE SETCE SECTORE	GLOBAL PROCEDURE GETFRAME FUNCTION: OBTAIN STORAGE FOR PAGE FRAMES. FUNCTION: OBTAIN STORAGE FOR PAGE FRAMES. TO THE WAXIMUM AMOUNT DESIRED BY THE USER. RETURNS TO CALLER WITH WUMBER OF FRAMES OBTAINED AND A POINTER TO THE START OF THE AREA.	ENTRY: RO= MAX NUMBER OF PAGE FRAMES DESIRED  RETURN RO= NUMBER OF FRAMES ACTUALLY OBTAINED  RI= BASE ADDRESS OF PAGE FRAME AREA  NOTE: ROUTINE WILL FAIL IF THERE IS NOT ROOM FOR AT  LEAST ONE PAGE FRAME PLUS SYSTEM SPACE (SYSFREE).  SPACE 5  EQU (4*1024) 4K FOR BUFFERS, ETC.
* * * * * * * * * * * * * * * * * * * *	EP 4 3 3	&CSECT	****	S * * * * * * * * * * * * * * * * * * *



EQU (4*1024+SYSFREE)  MINIMUM ACCEPTABLE AMDUNT  SPACE  O.12  O.5=A(SYSFREE)  SAVE MAX DESIRED AMOUNT  O.5=A(SYSFREE)  SAVE MAX DESIRED AMOUNT  SAVE AMOUNT  CONVERT PAGES TO BYTES  SAVE MAX DESIRED AMOUNT  SAVE AMOUNT  SAVE AMOUNT  CONVERT PAGES TO BYTES  SAVE AMOUNT  SAVE AMOUNT  (1701-SYSFREE)  ADD SYSFREE  ADD SY	ACE 1.GOTLIST  1.GOTLIST  0.GOTLIST+4 PLUS AMT FREED GIVES NEW BASE ADDR 0.GOTLIST+4 MINUS AMDUNT FREED GIVES NEW BASE ADDR 0.GOTLIST+4 MINUS AMDUNT FREED GIVES NEW FATEL 1.GOTLIST+4 DIVIDED BY 4096 GIVES NEW FATEL 1.A(COREMIN.O) A(COREMIN.O) A(COREMIN.O) ACE 5	**************************************	LC & CCSECT TRY & EEP ING
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GETFRAME * ABOVE	A SKLIST GOTLIST SAVE D	* 1 * * * * * * * * * * * * * * * * * *	а п п п



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DDNAME=PAGEFILE,MACRF=(WL),DSORG=PS,RECFM=F,DEVD=DA
5
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    BEFORE
SIZE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    NOTE: CALLING PROGRAM IS RESPONSIBLE FOR STOPPING
FILE SIZE IS EXCEEDED ($ 837 OR D37 ABEND). FILE
AND BLOCKSIZE DETERMINED BY DD CARD.
                                                                                                                                                           REGISTERS
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  OPEN??
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     14=RETURN ADDRESS
13=SAVE AREA ADDRESS
0=POINTER ID BUFFER CONTAINING RECORD TO
BE WRITTEN.
                                                                                                                                                           RESTORE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       CLOSE??
INITOCLOS
YES
INITDCB+DCBOFLGS-IHADCB, YES
INITWRIT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           GLOBAL PROCEDURES GETPAGE AND PUTPAG
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         INITDECB, SF, INITDCB, (2)
INITDECB
INITE XIT
MEND
SPACE
MACRO
EXIT
L4
14
DROP
12
MEND
ECSECT SETC . $PAGE.
$CSECT CSECT
$CCSECT CSECT
$CCSECT CSECT
$CCSECT CSECT
$CCSECT CSECT
$CCSECT CSECT
$CCSECT CSECT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       14=RETURN ADDRESS
13=SAVE AREA ADDRESS
10-DINTER TO BUFFER
1=PAGE NUMBER (0 -> N-1)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  (INITDCB, (OUTPUT))
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           SPACE 3

ENTER 2.0

BM INITOLOS

BOAC INITURE CB. (
SPACE INITOCB. (
SPACE SPACE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         I NI TCL OS
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GE ENTER

CLOSE 2

GE CLOSE PAGEECEB

BNG

GE CLOSE PAGEECEB

CLOSE PAGEECETIT

SPACE

SPACE

SPACE

CHECK PAGEDCB, (UPDAT)

CHECK PDECB1,DI, PAGEDCB, (2),'S',0,PAGENO+1

ENTER

SPACE

THE SPACE

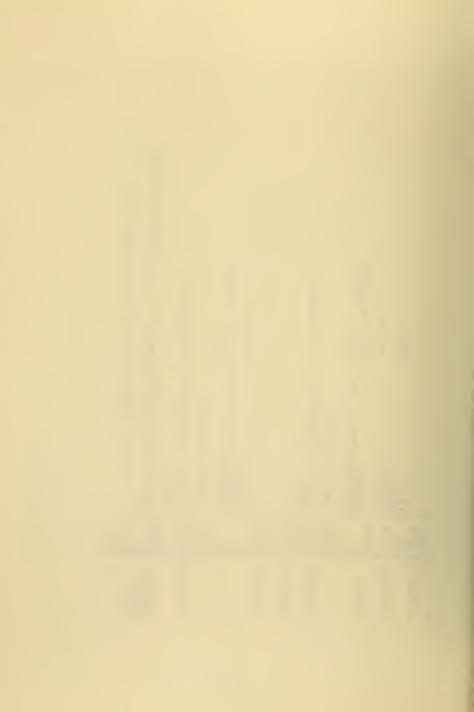
THE SPACE

CHECK PDECB1,DI, PAGEDCB, (2),'S',0,PAGENO+1

CHECK PDECB1

TO SPACE

THE SPACE
                                                                                                                                                                                                                                                                                           SAVE PAGENUMBER
PAGEDCB+DCBOFLGS-IHADCB,X'10' OPEN??
READPAGE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       2,0
CLOSPAGE
1,0405ENO
PAGEDCB+DCBOFLGS-IHADCB,X*10* OPEN??
WRITPAGE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         WRITPAGE
                                                                                                                                                                                 CLO SPAGE
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PAGENO
SAVE
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                                                                                                                                                                                                                                                                                                    GOPAGE
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### APPENDIX C

# JOB CONTROL LANGUAGE

//SYSUDUMP DD SYSOU //SYSIN DD \* (AN/UYK-7 PROGRAM DA



### APPENDIX D

### EXTENDING I/O CAPABILITIES

The limitations imposed by the IOC would prevent running a generalized program such as the ULTRA-32 assembler or CMS-2 compiler which would require more complex I/O facilities. The following paragraphs describe two approaches to extend the capabilities of the IOC. It is important to note, however, that while it might be possible to run a large program such as a compiler, this is not the primary purpose for an interpreter and the execution time would be excessive.

The first alternative would be to implement the additional channels available in the IOC for other devices (e.g., tape, disk or punch). This method, while providing realism, requires considerable knowledge of PL360 and the AN/UYK-7.

A more efficient alternative than the first would be to use external I/O routines. These routines may be either IBM System/360 routines or routines written in compatible languages. The method of invoking these routines will require modification of the interpreter program. One method is to use the 'Enter Executive State' instruction, opcode 07 with f2 of 0, to call the external routines. One bit of the 16 bit field contained in this instruction could be a flag indicating that external I/O was the desired operation.

The recommended method is to modify the code for the 'Initiate I/O' instruction to include the use of the a field. This field then would indicate whether the IOC or the external I/O routines were to be invoked.



This second alternative would also eliminate the requirement that the user write IOC programs to execute the desired I/O.

Anyone modifying the interpreter program must consider the following possible consequence. The single data segment, which contains all declared variables, has only 640 bytes of additional area available. If declarations are increased above this amount data segment overflow will result and considerable modification of the interpreter program will be necessary.



## CONTROL CARDS

HALT. PREVENT LOOPING BY ANY CPU

105 SHOT INTER-PROCESSOR INTERRUPT TO CPU 0

106 INITIATE 1/0 FOR READING A CARD

107 LOAD A(1)

108 LOAD A(1)

108 EQUAL TO SET FLAG BITS TO SORT

108 A(2)

108 EQUAL TO SET FLAG BITS TO SORT

108 A(2)

108 EQUAL TO SET FLAG BITS TO SORT

108 A(2)

108 EQUAL TO SET FLAG BITS TO SORT

108 A(2)

108 EQUAL TO SET FLAG BITS TO SORT

108 A(3)

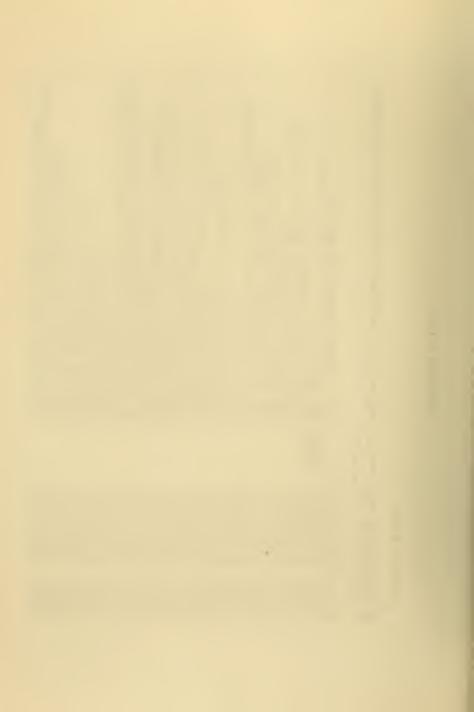
108 FROM Y(599)

108 EQUAL TO SEGNORY

108 A(3)

108 A(4)

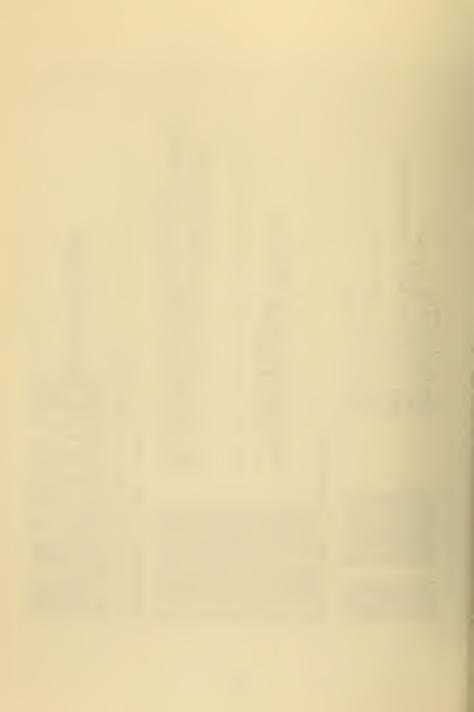
1 00013500014 ENT  $\begin{array}{c} \tt 000107000113 & \tt 000114000120 & \tt 000121000127 & \tt 000128000134 \\ \tt F1 \\ \tt 010000 & \tt 001031 \\ \end{array}$ 0000005 000100000106 000 201 PI PL 00120 000126 



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VALUE OF 2099
ONE IN SIGN POSITION
                            2
                                                                                                                                                                                                                                                READ/WRITE BUFFER
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A(1), 2100+(B(1)+1)
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LOBRO GUT A(1)
LOBRO GUT A(1)
LOBRO GUT A(1)
LOBRO E A(1)
LOBRO E A(1)
BRANCH E A(1)
BRANCH
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E TO TERMINATE
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EGISTER 1 WITH 130
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P REG FOR CPU 0 TO LOI
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                                   2100
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I/O METE INSTRUCTION
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TEST & SET (2049)
LUMP IF SET (2049)
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SWAP A (1) -> 2100 + (8(11)
B (1) -> 1705 | 2
3 UMP IF <= 1705 | 2
1 UMP IF <= 6 (1) LOAU
UNCOND TO LOAU
                                                                                                                   SS
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                                                                                                                                                                                                                   AT
                                                                                                                   VALUE
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MEMORY VAILABLE IS FOOD 003071
PROGRAM EXECUTION FOR CPU O WILL START
PROGRAM EXECUTION FOR CPU O WILL START
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MEMORY DUMP IS FROM 000107 TO 000106
MEMORY DUMP IS FROM 000127 TO 000108
MEMORY DUMP IS FROM 000127 TO 0001120
MEMORY DUMP IS FROM 000121 TO 000127
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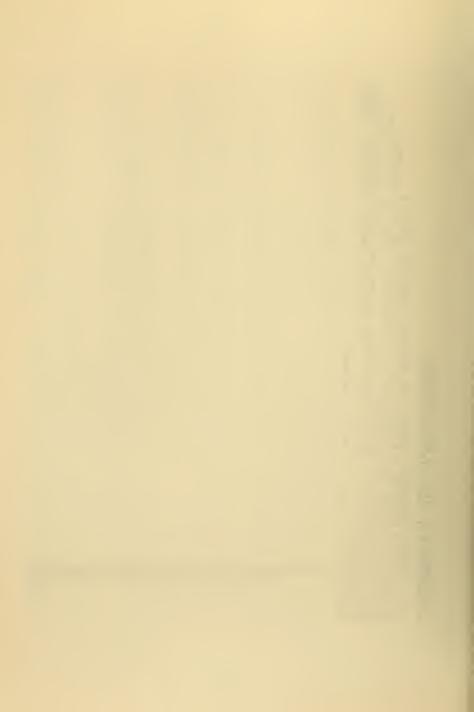




000 001 2049 307B 300000000 0000 : 0000011 0000007C HEX): 0000000 00000 4 000 000 200 15 HEX): 00000 č IMAL): IMAL): IMAL): MAL): ۵ŏ 4 IL 007 5 3758 8.. 0000 HEX): 0002 HEX): 00020 HEX) 00000 HEX) UE E CDEC I 07 SH OH EC. ش٥ шO 00  $\Box$  $\bar{\omega}$ صس FOR CPU # 0
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ER (IN HEX):
A VALUE (IN FOR CPU # 0
ER (IN HEX):
A VALUE (IN 0..Z #X ADDRESS (DECIMAL): 000122 IN INTERRUPT STATE FOR CPU # 0 STATUS REGISTER (IN HEX): 00010E06 P REGISTER (IN HEX): E: 77 ACCUMULATOR DESIGNATOR: 0 ACCUMULATOR DESIGNATOR: 0 I DESIGNATOR ON 0 .. Z шш**~** N INTERRUPT STATE FOR CPU # (0010606 P REGISTER (IN HEX) R: 2 ACCUMULATOR A VALUE (IN EFFFF A(B) VALUE (IN HEX): ш SS  $\supset \sim$ SS SS CPU# IN HEX AL. ES: ΔЩ ZШ NA REI >~ >~ >~ Spi 900 000 90 FOR A MA PE ΜĀ FD RE **m**⊲ -D RF <u>~</u> ٣ \_\_\_\_ TATE F GISTER ATOR A TATE F GISTER ATOR A UVK-7 ADDRESS (DECIMAL): 000124 IN INTERRUPT STATE FACTIVE STATUS REGISTER (IN MEX): 00053E00 P. REGISSER OF CODE: 24 ACCUMULATOR DESIGNATOR: 7 ACCUMULATOR ALINDEX DESIGNATOR: 7 ACCUMULATOR ALINDEX INDEX шШ шШ NTERRUPT STATE 3E00 P REGISTER 7 ACCUMULATOR шШ OMPUTE COMPUTE 1 BASE COMPUTE UVK-7 ADDRESS (DECIMAL): 000121 IN INTERUPT ST ACTIVE STATUS REGISTER (IN HEX): 00010E06 P REG OF GODE: 24 ACCUMULATOR DESIGNATOR: 2 ACCUMULA INDEX DESIGNATOR: 0 NO INDEX ING NO INDIRECT ADDRESSBASE REG DESIGNATOR: BASE 0 RASIG OPERAND ADDRESS (DECIMAL): 2049 FINAL COM R DESIGNATOR: 3 (Y) (IN HEX): FFFFFFF ACCUMULATOR A+1 VALUE (IN HEX): FFFFFFFF UVK-7 ADDRESS (DECIMAL): 000123 IN INTERRUPT ST ACTIVE STATUS REGISTER (IN HEX): 00053E00 P REG OP CODE: 10 ACCUMULATOR DESIGNATOR: 7 ACCUMULA INDEX DESIGNATOR: 0 NO INDEXING NO INDIRECT ADDRESSBASE REG DESIGNATOR: BASE 0 ACCUMULATOR: 0 (Y) (IN HEX): FC600000 ACCUMULATOR A+1 VALUE (IN HEX): 00000117 SE BA •• UVK-7 ADDRESS (DECIMAL): 000125 IN IN OP CIDE: 24 ACCUMULATOR DESIGNATOR: 7 INDEX DESIGNATOR: 0 ND INDEXING ND INDIRECT ADDRESSBASE REG DESIGNATOR BASIC OPERAND ADDRESS (DECIMAL): 0501 UVK-7 ADDRESS (DECIMAL): 000120 IN ACTIVE STATUS REGISTER (IN HEX): 0 ACCUMUATOR DESIGNATOR F4 DESIGNATOR: 2 ACCUMULATOR A+1 VALUE (IN HEX): FFI TIVE CODE DESI DAOT YOT4



(DECIMAL): 000000 DECIMAL): 000800 0000007E HEX): 00000117 ACTIVE STATUS REGISTER (IN HEX): 00053E00 P REGISTER (IN HEX): 00058: 07 ACCUMULATOR: 0 NO INDEXINATION: 0 NO INDEX STATUS (IN HEX): 000 INDIRECT ADDRESSBASE REG DESIGNATOR: 0 BASE REG VALUE (BASIC OPERAND ADDRESS (DECIMAL): 0800 FINAL COMPUTED ADDRESS (DECIMAL): 0404040 (Y) (IN HEX): 40404040 VALUE (IN HEX): 00000117 K DESIGNATOR: 3 ACCUMULATOR A+1



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		215021F3	916021F3	A5202000	1C400320	E586E430	ACA02024				
		ACA02014	2D7021F3	54340000	53B021F5	AF 202037	FOCE0000				
		90B0212C	AD2 02 007	4D10279C	53B021F4	8D10279C	ACA02033			IAL VALUE	000000000000000000000000000000000000000
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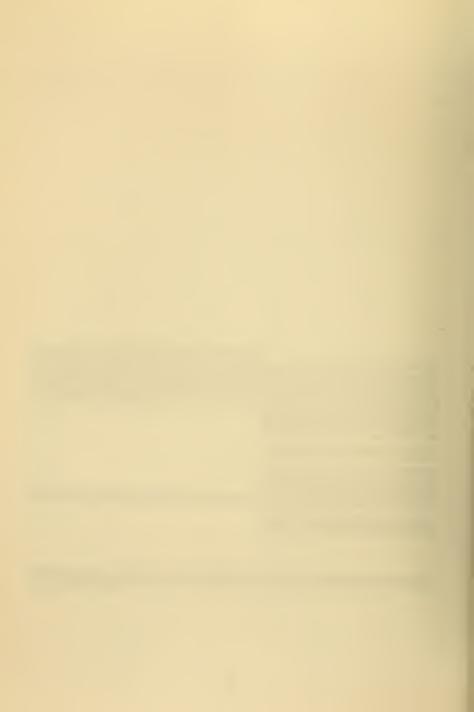
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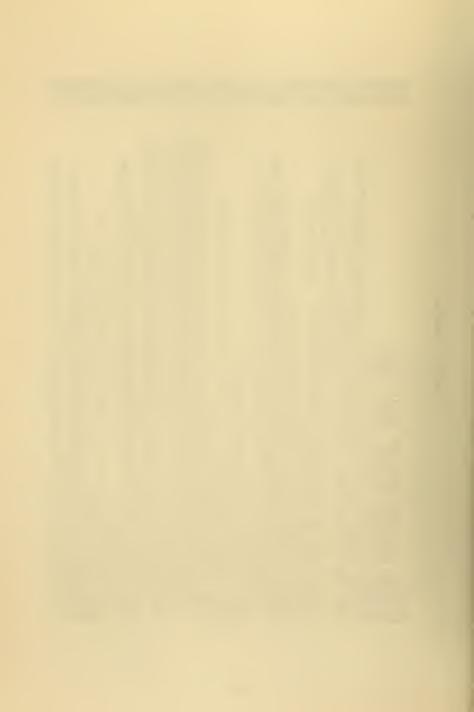


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\*\*\*\* END EXECUTION \*\*\*\*



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        TPAGE (R14); NULL;
TPAGE (R14); NULL;
TFRAME (R14); NULL;
TFRAME (R14); NULL;
NCTION BXLE(3,#8700); FUNCTION
TION ALR(1,#1500); FUNCTION
0=(25(0),#10600,8(0),1,75(0),
0=(25(0),410600,8(0),1,75(0),
75(0),75(0),
340),CPUZ SYN CPUO(680);
SYN R9, CPUBASE SYN R11, OP
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BRANCH (R14)

KECREMOTE TUP: PEOUT;

SEX

PROCE DURE CASE RI CASE RI BEGIN BEGIN COTO S COTO S END:

2 ACCORDING INSTRUCTION RESET(INDEX) ADDRESS (8(8)) FINISH; Z + ERAND PROCEDURE COMPUTESPECY (R14);

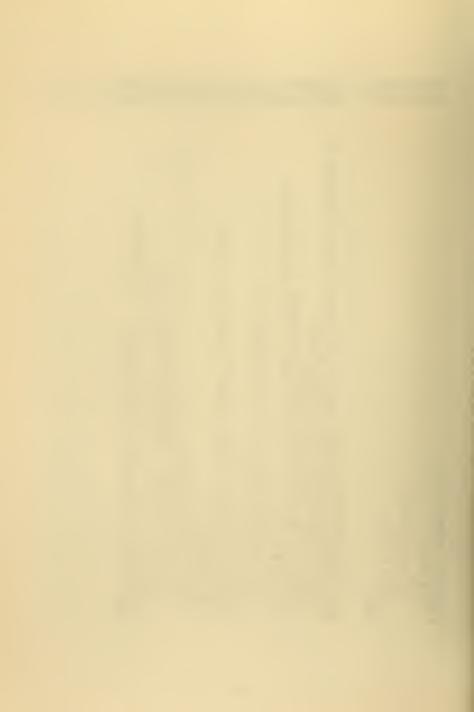
BEGIN COMMENT THIS PROCEDURE COMPUTES THE OPERANC ARRAY 2 INTEGER REGSAVYCOM;

SAV14: SAV14: STAKENDE FECTANDE FORMAT;

SAV14: STAKEND FEFF;

SAV14: SAV14: STAKEND FEFF;

SAV14: SAV SS: R3 ...× H GLOC := R3 COMMENT



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01008
01100
01111
001112
01113
PROCEDURE COMPUTEY (R14):

BEGIN COMMENT THIS PROCEDURE COMPUTES OPERAND ADDRESS Y BY ADDING Y +

BEGIN COMMENT THIS PROCEDURE COMPUTES OPERAND ADDRESS Y BY ADDING Y +

INTEGER SAV14:

INTEGER REG SAVCOM:

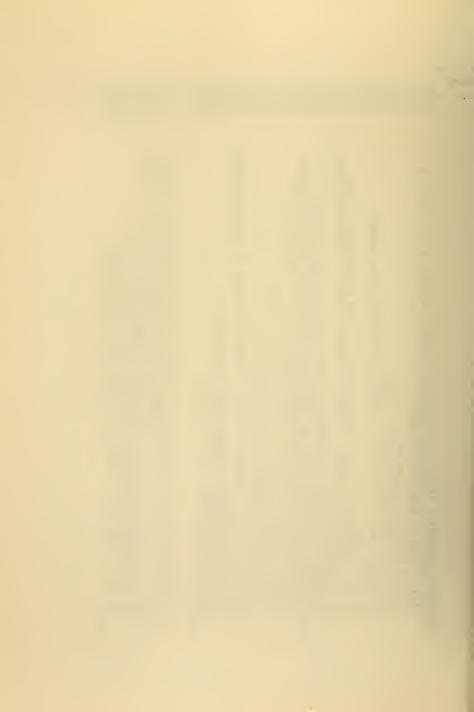
STR (R3,R4,REG SAVCOM):

SET (INDEX):

SET (INDEX REG SAVCOM):

SET (INDEX REG SAVITA:

SET
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             R2 AND R3 AND RETURNS VALUE IN R6
SETS FIXED POINT OVERFLOW IF NEEDED
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THEN
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ALSO
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           C = ASR AND #FFFFFF7; R6 := 0VERFLOW OR > THEN R6 := R6 + R2 > 0 AND R3 > 0 AND R6 > 0 T
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             COMMENT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               ADD (R14)
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|                                                                                                                                               | COMMENT K =                                                                                                       | A Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y | 00000<br>00000<br>00000<br>000000<br>000000<br>0000000                                                                     |                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|
| PROCEDURE NORMREAD (R14): BEGIN COMMENT USED FOR OPCODES 10 - 47; ARRAY 3 INTEGER SAVEI4: SIM(R2:R4:SAVENREAD): SAVE14:= R14; R6:=R6+1: BEGIN | BEGIN<br>R3 := ASR; R2 := INDEXREGVAL AND #FFFF;<br>R3 := INST SHLL 16 SHRA 16; ADD;<br>ASR := R4; R6 := OPERAND; | OPERAND := OPERAND SHLL 16 SHRA 16;     | OPERAND := OPERAND AND #FF;<br>OPERAND SHL 8 AND #FF;<br>OPERAND := OPERAND SHR 16 AND #FF;<br>OPERAND := OPERAND SHRL 24; | LM(R2,R4,SAVENREAD); R14 := SAVE14;<br>END; |

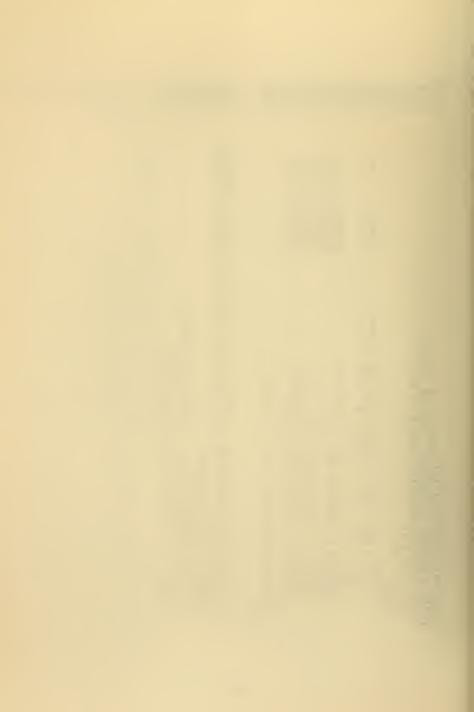
PROCEDURE WRITES A STRING THE REGS & BLANKS THE WBUF; MVC(131, WBUF, BLANK); WBUF & RESTORES OF WRITSTRING PROCEDURE WRITSTRING (R14);

PREVIOUSLY PUT IN THE W
BEGINT:

ARRAY 4 INTEGER REGWRIT;

STM(R14,R1,REGWRIT);

R0 := 20WBUF; WRITE; M
R(R14,R1,REGWRIT);
ENO:



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NO
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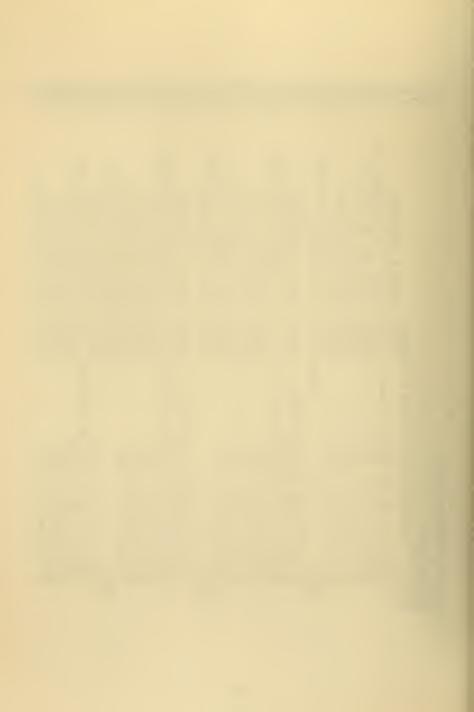
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NTERRUPT



COMMENT LOAD THE P REG: COMMENT END CLASS 4 INTERRUPT; BRANCH; COMMENT END INTERRUPT; END: COMMENT END OF CASE END: = R3;
END: COMMENT END OF CASE END:



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OUTSIDE

MEMORY ACCESSES

INTERRUPT (R14); UP INTERRUPT CALLS FOR

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PROCEDURE COMMENT

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EGMENT PROCEDURE MEMORY (R14);
COMMENT SIMULATES ANVUYK—7 MEMORY. THIS PROCEDURE ACCOMPLISHES
ALL MEMORY ACCESSES AND DOES PAGING OF THE SIMULATED ANVUYK—7
MEMORY AS REQUIRED BY THE CPU AND IOC;
EGIN ARRAY 9 INTEGER REGSAVEM; INTEGER SAVE14;
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     60:
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                                                                                                                                                PROCEDURE FETCHPAGE (R14);

BEGIN MITEGER SAVELE;

SAVEIL;

SAVEIL;

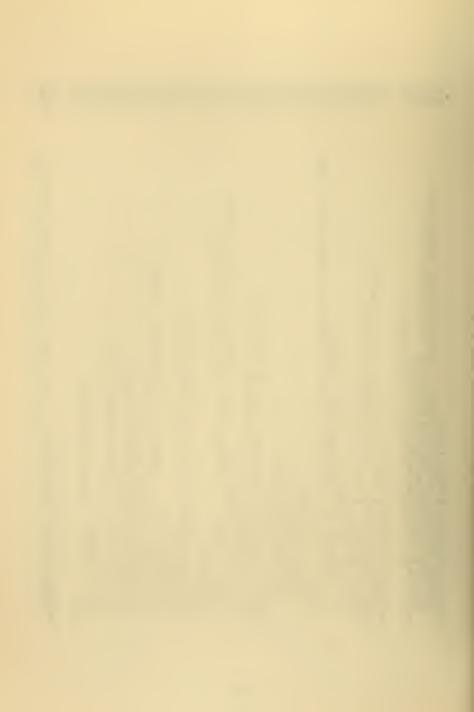
SAVEIL;

SAVEIL;

SAVEIL;

SAVEREGS;

SAVEREGS;
                                                                                                                                                                                                                                                                                                             MASK
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     COMMENT R1 = PAGE #
PAGE, MUST WRITE OUT
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                                                                                                                                                                                                                                                                                             PAGE
                                                                                                                                                                                                                                                                                                                                     ••• \
                                                                                                 MEMORY
                                                                                                                                                                                                                                                                                                                                   PAGE 3
                                                                                                                                                                                     RETURN VALUE
                                                                                                                                                                                                                                                                                             FOR
                                                                                                                                                                                                                                                                                                                                   COMMENT R3 =
                                                I INSTRUCTION FETCH CASE;
T OPERAND FETCH CASE;
T IOC MEMORY FETCH;
T IOC MEMORY STORE;
T UNCONDITIONAL NORE;
I NOINECT ADDR FETCH;
                                                                                                                                                                                                                                             COMPUTE 360 ADDRESS
B8; GOTO ENDFETCH;
                                                                                                                                                                                                                                                                                            ENTRY
                                                                                                                                                                                                                                                                          ••
                                                                                                                                                                                                                                                                         SHLL 1;
NE #;
ABLE ENT
                                                                                                                                                                                     DDRESS IN R5, R SAVEREGS;
   SAVEREGS
                                                                                                                                                                                                                                                                         COMMENT R2 = PAGE #
COMMENT R5 = LI
COMMENT R3 = T,
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R
  /E14; ARRAY 9 INTEGER S/
STM(RO, R8, SAVEREGS);
SHLL 4; RI := MEMCASE
                                                                                                                                                                                                                                                                                                                                   COMMENT
MEMBASE
                                                                                                                                                                                                                                             BYPASS PAGING AND (+ MEMBASE; R8 := 1
                                                                                                                                                                    PROCEDURE MEMFETCH (R14);

COMMENT FETCH THE AN/UYK-7 MEMORY AD
BEGIN INTEGER SAVE14; STM(R0,R7,SAVERGS);

R14:= MEMLIMIT: STM(R0,R7,SAVERGS);

R14:= MEMLIMIT: STM(R0,R7,SAVERGS);

R5 >= R14 THEN MEMINTERUPT;

IF TO PAGIN SHIPS SPACING AND
R8 := R5 SHL 2 + MEMBASE; R8 :=

RD:
R8 := R5 SHL 10 SHLL 1; COMMENT R
R9 := R5 SHL 2; COMMENT R
R5 := R5 SHL 2; COMMENT R
R5 := R3 AND #COFF;

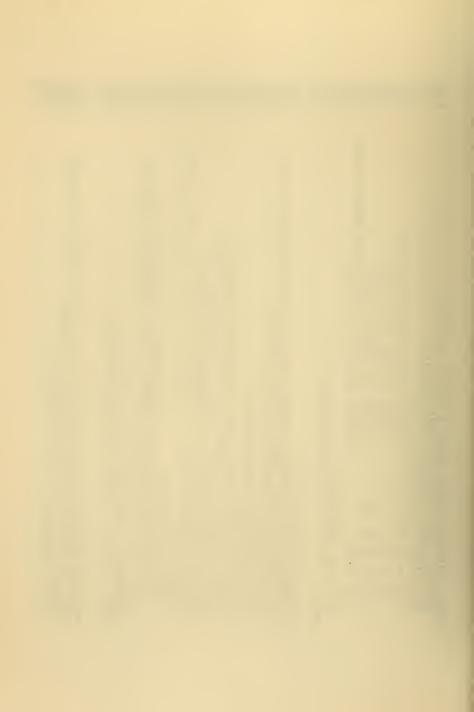
PAGETABLE (R2);

R4 := R3 AND #COFF;

R6 := R3 AND #COFF;

R8 := R3 GOTO ENDFETCH;

FFT CHPAGE; GOTO SETR3; LM(R0,R7,S) ENDFETCH; R14 := SAVE14; LM(R0,R7,S)
                                                                                                                                                                                       SEE
                                                                                                                                       8, SAVEREGS)
                                                  0, R
                                                                                                                                •••
                                                                                                                              RRUPT:
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ACI

ADDR 3.E EAKPOINT DIS EAKPOINT WITH B  $\alpha$ В SE SE ••• NOPROCK; SPR; ENTS WITH S Sa CEMENT: R2:= 14: INTERRUPT: END: 2: COMMENT R5 = UYK-7 ADDR: E + 96) SHLL 13: COMMENT R2 HA S DDRE SAVE14 := R14; STM(RO, RB, REGSAVEM);

CASESTART:CASE R1 DF

BEGIN

R2 := R7 AND #FFFF;

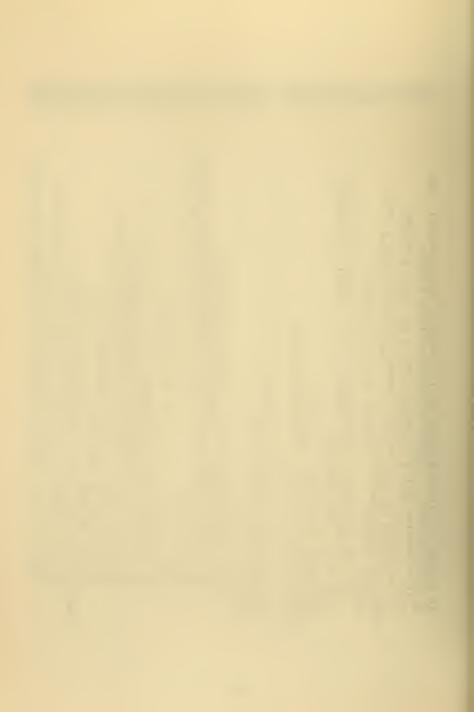
COMMENT R3 := R7 AND #FFFF;

COMMENT R3 := R1 COMMENT B1 I I OF ASR IN R5 := R1 COMMENT B1 COMMENT B2 SPR CONTENTS R5 := R1 COMMENT R5 = R1 COMMENT B1 COMMENT R5 END;

COMMENT R5 := R1 COMMENT R5 = R1 COMMENT R5 END;

COMMENT R5 := R1 COMMENT R5 = R1 COMMENT R5 END;

COMMENT R5 := R2 SHLL I SHRL I SHRL I SCOTALING END EAKPOINT AI COMMENT INSTRUCTION FETCH:
MEM(CPJBASE + 328);
COMMENT R2 = DISPLA(R7 AND #FFF;
COMMENT R2 = DISPLA(R7 AND #E0000 SHRL 17 SHLL 2; COMMENT STRLL 20; COMMENT STRLLL 20;



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BRANCH;
                                                                                 COMMENT LOAD
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:= B5; COMMENT
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ASR AND #400;

O OR EXECSTATE THEN GOTO NOCHK;

BASEREGLOC + 200; R5 := B5; COMMENT

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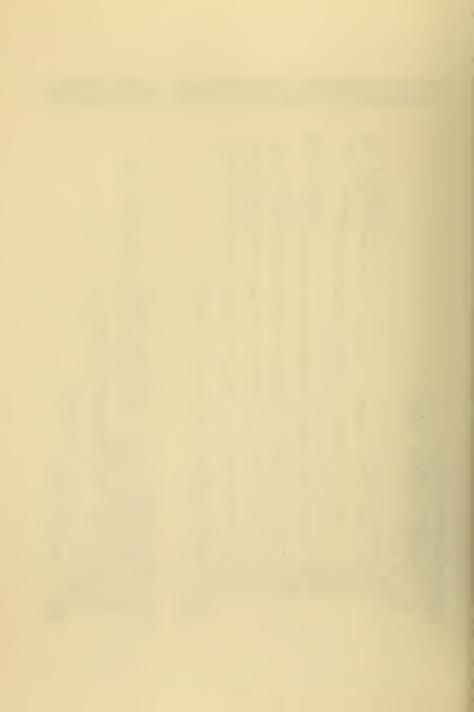
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RO := AMBUF; WRITE: MVC(60.WBUF.BLANK); RT := #F0;

RO := AMBUF; WRITE: MVC(60.WBUF(61));

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COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

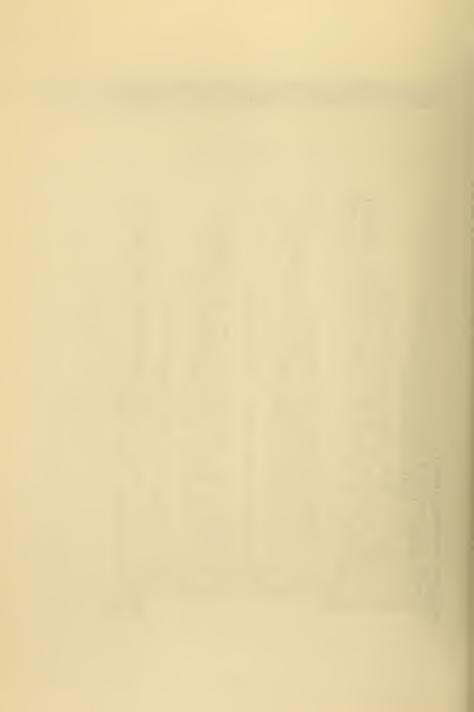
COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

COUTOUT: RO := AWBUF; WRITE: MVC(60.WBUF.BLANK); RI := RI + 11

END:

COUTOUT: RO := ATER RO := AVEIL4; RO 
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               d ...
= R11, A
= R11, A
= > R2,
MEM(R4);
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SCALE
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MEM(R4)
R2 --> M
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4 IN R7
3 FETCH
4 STORE
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7;
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OR #(
                    AKK
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                                                        BEGIN

ARRAY 1 INTEGER 1CBUF SYN GBUF;

ARRAY 1 S INTEGER 1WBUF SYN WBUF;

ARRAY 1 LINTEGER 1WBUF SYN WBUF;

BYTE CHAIN, MOTOR CAR;

GET: 8 = 3 MEMONY;

GET: 8 = 1 NST SHR 26 - 7;

GOT: 0PCODE = 1 NST SHR 26 - 7;

GOT: 0PCODE = 1 NST SHR 26 - 7;

GOT: 0PCODE = 1 NST SHR 26 - 7;

GOT: 1 S SAVIO);

END: 0PCODE = 1 NST SHR 28;

RS = 1 NST SHL 8 SHR 28;

RS = 1 NST SHL 12;

IN ST SH  SHR 28;

RS = 1 NST SHL 12;

IN ST SH  SHR 28;

RS = 1 NST SHL 12;

IN ST SH  SHR 28;

RS = 1 NST SHL 12;

IN ST SH  SHR 28;

RS = 1 NST SHL 13;

RS = 1 NST SHL 14;

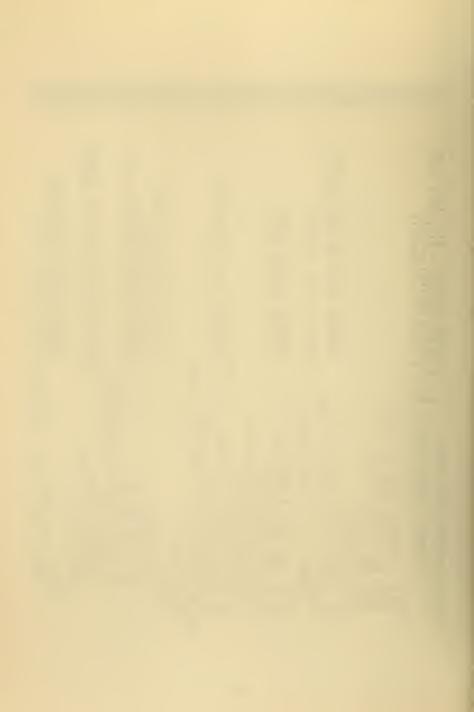
IN ST SH  SHL 6 SHR 13;

RS = 1 SS SHL 14;

RS = 1 SS SH  SHR 13;

RS = 1 SS SH 13;

R
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                                  ••
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 EGMENT PROCEDURE I OC (R14)
                                MEMORY
                              COMMENT
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NO EXTERNAL FUNCTION 12:
NO EXTERNAL INTERUPT 13:
NO EXTERNAL INTERUPT 13:
INTERPUPT OPCODE 14:
GET CP NO:
SHIFT FOR LOCKOUT REG.:
CHECK FOR ENABLE ON CH.J;
        FOR GUTPUT;
COMMENT 100 FERD IN REST OF COMMENT SET OPECODE:

FOUTO STARTIO:

COMMENT SET OPECODE:

RI := ASR SHR L 20 SHLL 1:

COMMENT OF FRAINATE INTERRUPT:

RI := ASR SHR L 20 SHLL 1:

COMMENT OF FRAINATE OPECODE OF SITE OF SET 
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   FIELDS;
R3;
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 OCMEM;
```



|                                                   | COMMENT ILLEGAL CAR OR CAP INST 21;<br>COMMENT GET CP NO.; | R6 := #07;                                                                           | COMMENT LOAD IOCMEM 22;<br>COMMENT MOD KJ FIELD TO INDEX CM;             | COMMENT LOAD RTC 23;<br>COMMENT STORE IOCMEM 24; | COMMENT STORE RZ IN MEM(R4);          | COMMENT SETBIT 25;               |                             | COMMENT SET BIT IN (Y);<br>COMMENT STORE (Y) MODIFIED;                       | COMMENT CLEAR BIT 26; | STARTIO: END:<br>COMMENT COMBINE KJ FIELD:<br>COMMENT GET I IN KJ BIT;         | COMMENT STORE BACK IN MEM(R4);             | COMMENT TEST & SET 27;<br>COMMENT BIT 31 SET; | COMMENT UPDATE OPERAND;              |
|---------------------------------------------------|------------------------------------------------------------|--------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------------------|---------------------------------------|----------------------------------|-----------------------------|------------------------------------------------------------------------------|-----------------------|--------------------------------------------------------------------------------|--------------------------------------------|-----------------------------------------------|--------------------------------------|
| END: 18 R3; GOTO GOT: END END ELSE GOTO ENDCHAIN: | SHLL 4:                                                    | ECTIVE S 15 THEN R6 := #06 ELSE R1 := R5 SHLL 5 OR R6; END: END: R1 := 3; INTERRUPT; | BEGIN<br>BEGIN<br>R6 := R6 SHLL 4 + R5 SHLL 3 + 4;<br>LIOCMEM(R6) := R3; | + R5 SHLL 3 + 4;                                 | R2 := IOCMEM(R6):<br>R1 := 4: MEMORY: | BEGIN<br>BEGIN<br>IF RG > 1 THEN | DPCODE := 10; GOTO STARTIO: | RD := R6 SHLL 4 OR R5;<br>R2 := 1 SHLL R6 OR R3;<br>R1 := 4; MEMORY;<br>END; | 7 1                   | BEGIN OPCODE := 14; GOTO STARTIO<br>R6 := R6 SHLL 4 OR R5;<br>R1 := 1 SHLL 46; | RZ := I AOR KI AND K3,<br>RI := 4: MEMDRY: |                                               | OPERAND := OPERAND + 1;<br>GOTO GET; |



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                                                                       MOD I
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COMMENT SAVE POINTER TO IOCMEM WORD
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                                                                                                                                                                                                                                                                                                    NEXT
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DATA TRANSFER;
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DATA SUPPRESS
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                                        SET BIT STORE OPE
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GET ADDR
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COMMENT SCALE
                                                                                                                       END
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CASE R5 OF

BEGIN

NULL: NULL:

BIGIN6 = 0 Th

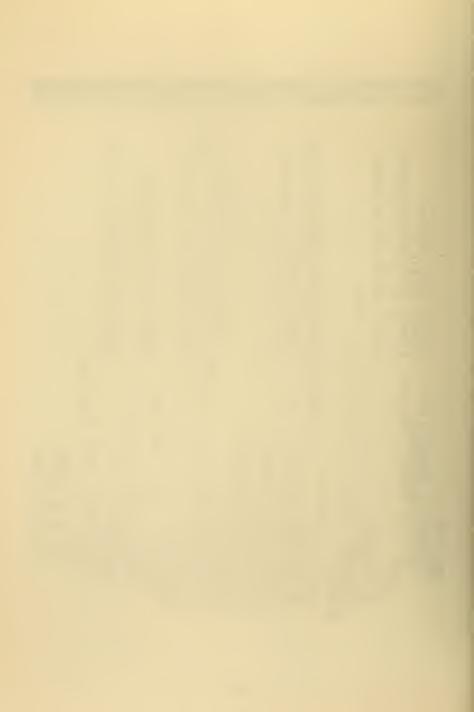
BEGIN = 0 Th

BEGIN = 20CMEM(44)

FOR PR := R3

FOR PR := R4

FOR PR := R4
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                NULL:
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) :=
                                                                                                                                                                                      OPCODE
= R2;
                                                                                                                                                                                                                                      COMMENT
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END ELSE
BEGIN ELSE
BEGIN RZ := 4:
END:
END:
END:
IF CHAIN THEN
GOTO DONG:
BUFFERI:
BUFFERI:
RI:
BUFFERI:
RI:
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EADER;
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CH 6 PRINT
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                                                                                                                                                                                                                                                           := INTLOCKOUT (R2) AND
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          COMMENT R2<- MEM(R4);
+ 4; COMMENT LOAD WBUF
                                                                   END
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CASE FOR
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                                                                   88
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         STORE
                                                                                                                                                               STORE
BEGIN RO := aCBUF; READ; RB := R7

END:= R7 SHLL 16 OR R4:

COMMENT S

END:= R7 SHLL 16 OR R4:

COMMENT S

END:= R7 SHLL 16 OR R4:

COMMENT S

END:= R8 SHRL 20 SHLL 1: R1 := IM

R2 := ASR SHRL 20 SHLL 1: R1 := IM

R2 := ASR SHRL 20 SHLL 1: R1 := IM

END:= ASR SHRL 20 SHLL 1: R1 := IM

END:= ASR SHRL 20 SHLL 1: R1 := IM

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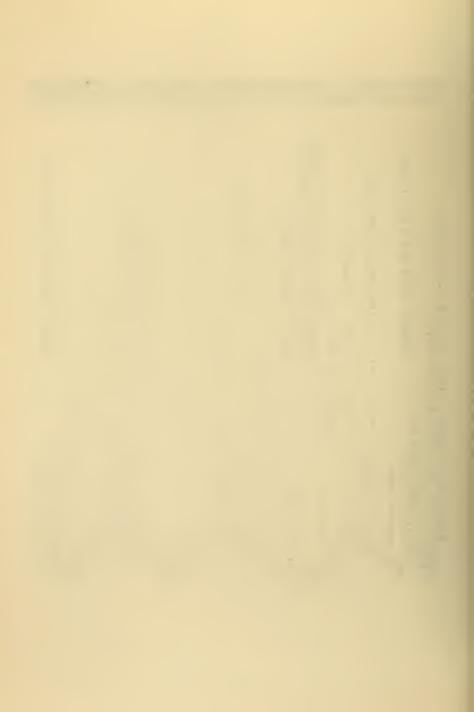
END:= ASR SHRL 20 SHL 1: R1 := IM

END:= ASR SHRL 20 SHL 20 SHL 1: R1 := IM

END:= ASR SHRL 20 SHL 1: R1 := IM

END:= ASR SHRL 20 SHL 20 SHL 1: R1 := IM

END:= ASR SHRL 20 SHL 
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R...
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= R7 :
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1180):=
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R7 I OCMEM (1)
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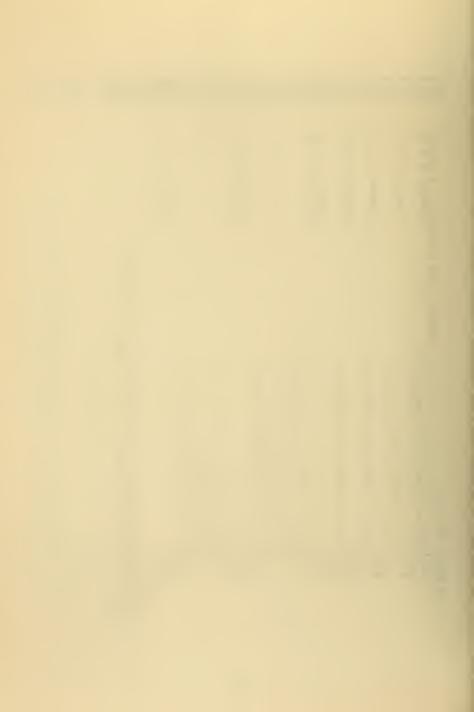
```
:= INTLOCKOUT(R2) AND #40;
                                    NULL: NULL: NULL: NULL: NULL: CHANNELL 7 15: CASE ON CH NO.;
                 INTERRUPT
                                                         COMMENT GET CAP;
                 #6E;
                 8 OR
    R1
```



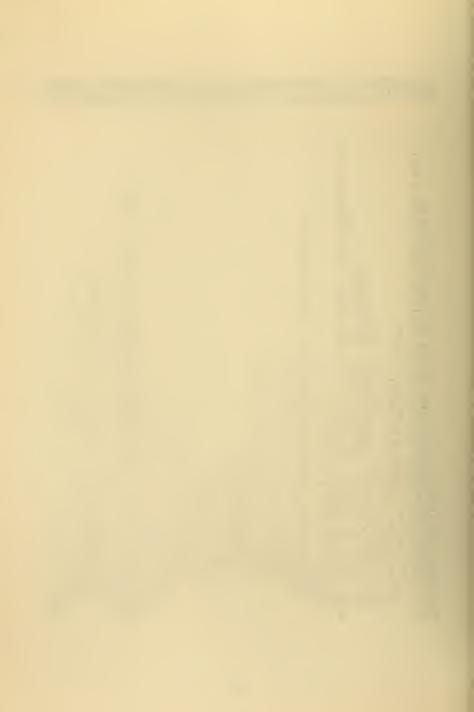
|                                                                                                                              |                                                                                                                                | VIION;                                              | JF SPECIAL A VALUE;<br>COMMENT A = 0; |                                | COMMENT A = 1;                         |                                         | COMMENT A = 2;                                                | COMMENT A = 3; |                                                       | COMMENT A = 4;               |                                | COMMENT A = 5;                       |                                            | CDMMENT A = 6;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | COMMENT A = 7: | •                                                    |        | R4 := 0;                                                                                                                                                                |  |
|------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|---------------------------------------|--------------------------------|----------------------------------------|-----------------------------------------|---------------------------------------------------------------|----------------|-------------------------------------------------------|------------------------------|--------------------------------|--------------------------------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| PROCEDURE REPEATTERM (R14);<br>COMMENT THIS PROCEDURE CHECKS FOR REPEAT<br>INSTRUCTION TERMINATION BASED ON SPECIAL A VALUE; | BEGIN<br>INTEGER SAV14: ARRAY 3 INTEGER REGSAVTERM;<br>SAV14 := R14: STM(R2,R4,REGSAVTERM);<br>R2 := RFPEATAVAL: R2 := R2 + 1; | BEGIN COMMENT CHECK FOR COMPARE INSTRUCTION TERMINA | COMMENT CASE C<br>BEGIN               | IF R3 = 0 THEN GOTO TERMINATE; | BEGIN<br>BEGIN<br>BEST := AVB AND #04: | IF R3 -= 0 THEN GOTO TERMINATE;<br>END: | BEGIN:<br>R3:= ASR AND #06;<br>IF R3 = 0 THEN GOTO TERMINATE; | END:<br>BEGIN  | R3 := ASK AND #OZ;<br>IF R3 -= 0 THEN GOTO TERMINATE; | BEG1N<br>R3 := A SR AND #02: | IF R3 = 0 THEN GOTO TERMINATE; | BEGIN<br>BEGIN<br>R3 := ASR AND #06: | IF R3 7= 6 OR R3 7= 0 THEN GOTO TERMINATE; | BEGIN<br>BEGIN<br>BEGIN<br>BEGIN<br>BEGIN<br>BEGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>BERGIN<br>B | BND:           | Rân:= ASR AND #01;<br>IF R3 = 0 THEN GOTO TERMINATE; | ENDIA. | END ELSE<br>BEGIN COMMENT CHECK FOR NON-COMPARE INSTRUCTION TER<br>R3 := ASR SHL 21; IF R3 < 0 THEN R4 := 104 ELSE<br>R3 := INST AND #3800000 SHRL 21 + CPUBASE + R4; F |  |



| COMMENT CASE OF SPECIAL A VALUE;<br>COMMENT A = 0; | COMMENT A = 1;                                            | COMMENT A = 2;                                                                      | COMMENT A = 3;                                  | COMMENT A = 4;<br>COMMENT A = 5;                                           |                                       |                                                                                    | COMMENT A = 6;                  |                                         |                                                  |                                                         | COMMENT A = 7; | RESET(REPLACE);<br>14;                                                                                                             |
|----------------------------------------------------|-----------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------|----------------------------------------------------------------------------|---------------------------------------|------------------------------------------------------------------------------------|---------------------------------|-----------------------------------------|--------------------------------------------------|---------------------------------------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------|
|                                                    | IF R3 == 0 THEN GOTO TERMINATE;<br>END;<br>BEGIN<br>BEGIN | IF K3 = 0. THEN GOLD TERMINATE;<br>END;<br>BEGIN<br>IF R3 >= 0 THEN GOTO TERMINATE; | END:<br>BEGIN<br>IF R3 < 0 THEN GOTO TERMINATE; | END:<br>NULL:<br>BEGIN<br>RZ := RZ - RZ;<br>FOR R4 := 0 STEP 1 UNTIL 31 DO | BEGIN<br>IF R3 < 0 THEN R2 := R2 + 1; | END: RZ := R3 SHLL I;<br>END: RZ := RZ BDD #01;<br>IF R2 := 0 THEN GOTO TERMINATE; | END:<br>BEGIN<br>R2 := R2 - R2: | FOR R4":= 0 STEP 1 UNTIL 31 DO<br>BEGIN | IF R3 < 0 THEN R2 := R2 + I;<br>R3 := R3 SHLL I; | END: R2 := R2 AND #01:<br>F R2 = 0 THEN GOTO TERMINATE; | ENDULL:        | END: FINISH: GOTO FINISH: TERMINATE:RESET(REPEAT): RESET(COMPARE): RESET(REPLACE); FINISH:LM(R2,R4,REGSAVTERM): R14 := SAV14; END: |



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3;
DUMP(R3+4);
       CARD
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   AND CMR REGISTERS AS
REGISTER DUMP CONTROL
                                                       SETZONE(WBUF(5));
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                                    BIL
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                                    A &
                         WREG;
WRITSTRING;
WRITSTRING;
R12 := 1;
GOTO WREG;
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                                                                                                                                                     STC(R3, WBUF (26))
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                                                                                                                                  WMEM;
240;
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           EGDUM
ROCEDURE DUMPS MEMORY
DUMP CONTROL CARD AND
PROCEDURE DUMP (R14)
BEGIN COMMENT THIS P
SPECIFIED BY MEMORY
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168;
= 88;
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CVD(R2,SAVEX); UNPK(5,7,WBUF(30),SAVEX);

WRITE: MVC(35,WBUF,BLANK);

:= II: IC(R1,NCPU); R3 := #F0;

UNTIL R1 D0
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        20
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     F || 82
                                                                                                                                                                                                                                                                                                                                                                                                                   VIRTUAL PAGES ARE");
EX); UNPK(2,7,WBUF(32),SAVEX);
MVC(34,WBUF,BLANK);
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         ⋖
                                                                                                                                                                                                                                                                                                                       AVEX )
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                                                                                                                                                                        CONFIGURATION")
SEGMENT PROCEDURE INITIALIZ2 (R14);

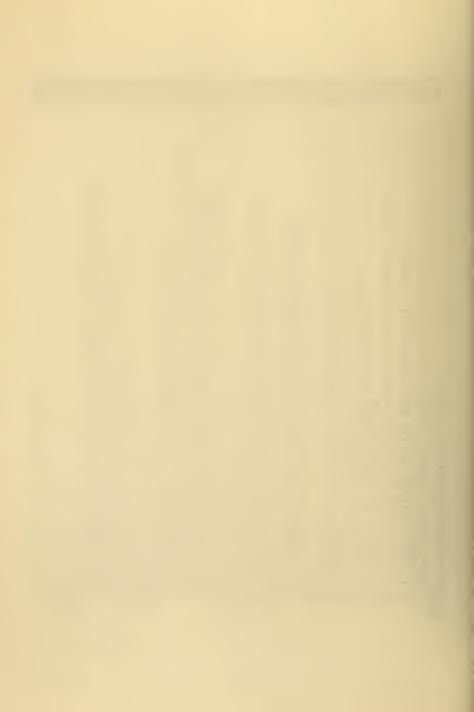
ROTE = AMBUF; WRITE = VE14 := R14;

ROTE = AMBUF; WRITE = VE14 := R16;

ROTE = AMBUF; WRITE = VE14 := R16;

ROTE = ROTE = R16;

ROTE
                                                                                                                                                                                                                                                                                                   2),54
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SETZONE (WBUF(29));
SETZONE (WBUF(39));
+ 8;
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          WR I TE
BEGIN

R5 := TRACEVAL(R2): R6 := TRACEVAL(R2 + 4):

R5 := TRACEVAL(R2): R6 := TRACEVAL(R2 + 4):

R6 := TRACEVAL(R2): UNPK (5,7*WBUF (24):SAVEX):

CVO(R6:SAVEX): UNPK (5,7*WBUF (24):SAVEX):

STC(R3:WBUF (14)): R3 := R3 + 1: R2 := R2

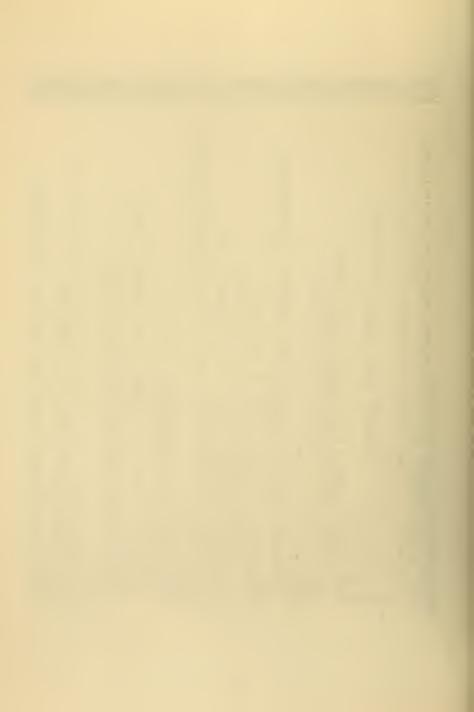
WTO (11:WBUF (14):WBUF (14):SELANK): WRITE:

WYC (21:WBUF (14):WBUF (15):WBUF (15):
                                                                                                               4
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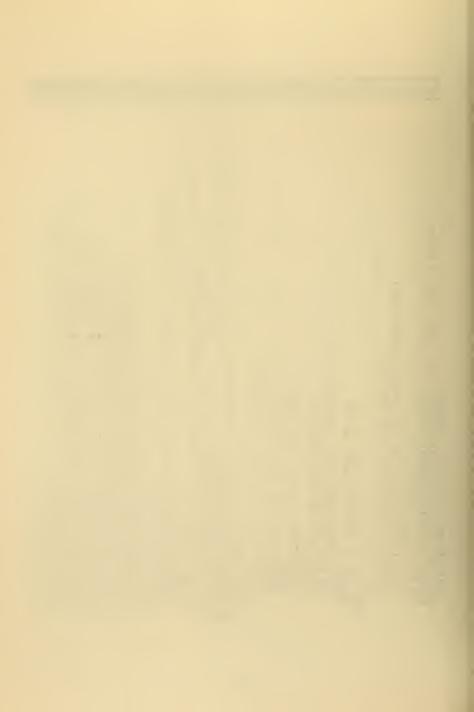


VIRT PAGES THEN PAGING=FALS REGISTER FLUSHED") 8 FLUSHED") SEGMENT PROCEDURE INITIALIZE (R14):

BEGIN INTEGER SAVE14:
SAVE14:=R14:
CONTROL CARDS"): WRITSTRING:
R5 := 1:
R6 := 3CBUF:
R6 := 3CBUF:
R6 := 3CBUF:
R7 := 3CBUF:
R6 := 8CBUF:
R6 := 8CBUF:
R7 := 8CBUF:
R8 := 8CBUF:
R9 := 8CBUF: R2 108 ı J08 ı !! PPAGES CPU'S SPECIFIED INCORRECT BRANCH; CORE 0 IC(R2, CBUF); WRITSTRING; SUPPL IED CARD END: END: RO := aCBUF: READ: IF > THEN GOTO EDF: IC(R2,CBUF(1)): MVC(79,WBUF,CBUF): BEGIN CONTROL MEMORY 4.WBUF, "NO VC (4



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                                                                                      PART IAL
                                                                                                   WRI TSTRING
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                                                                                                              FL USHED"
                                                                                      CARD
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    acBUF
                                                                       BUF (R6
                                                                                      MEMORY CONTROL
                                                                                                                                         2;
                                                                                             ; := R2 - R2; IC(R2,CBUF);
2,CBUF(1)); MVC(79,WBUF,CBUF);
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                 5 = #40 THEN G
B(R2, SAVEX);
R4 XOR _1; R1
                                             7
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    S
                                             := MDUMP(R2
NEXTA:
R6 THEN
    œ
NCH;
R3;
                                                          WSTA
                                                                 THEN
                                   MEMLIMIT; R7 := 1;
0 STEP 8 UNTIL 40 DO
RA = 4
STRING; R1 := 3;
R3 := R3 - R3; R4
:= 3 STEP 7 UNTIL
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REGISTER CONTROL CARD PARTIAL
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  SIGN FOLLOWING");
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IF R2 -1= "%" THEN GOTO BEF: R2 := R2 - R2: IC(R2,CBUF):
IF R2 -1= "%" THEN GOTO BEF: R2 := R2 - R2: IC(R2,CBUF):
IF R2 -1= "%" THEN GOTO BEF: R2 - R2: IC(R2,CBUF):
BEGIN WRITSTRING: R1 := 3: BRANCH:
END: WRITSTRING: R1 := 3: BRANCH:
COMMENT START READING INSTRUCTION CARDS AT THIS POINT:
R0 := 3MBUF: WRITE: WRITE: WRITE: WRITE: WRITE: WRITE:
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   ...
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BEGIN

EXTENDED

EXTENDED

EXARTDUMP:

IF R2 > 130 THEN R2 := 130;

IF R2 > 130 THEN R2 := 130;

IF R2 > 130 THEN R2 := 130;

ENDOWNP := R2;

ENDOWNP := R3;

ENDOWNP := R3 + R4;

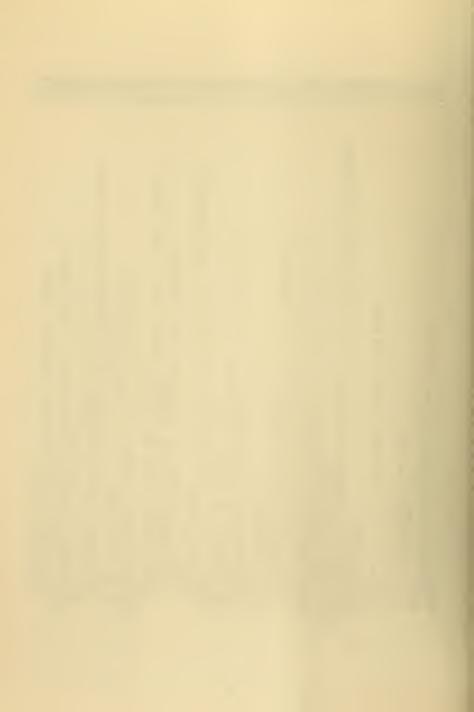
ENDOWNP := R4 + 5;

ENDOWNP := R4 + 7;

ENDOMNP := R4 + 7;

ENDOWNP := R4 + 7;

ENDOMNP := R
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              R8
                                                                                                                                                                                                                                                                                                                             GOTO WSTB
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GOTO ST
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        UNPK(5,7,WBUF,SAVEX);
                                                                                                                       BEGIN

WYC(79.WBUF(8),CBUF);

END:

RI = R12; IC(R1,CBUF);

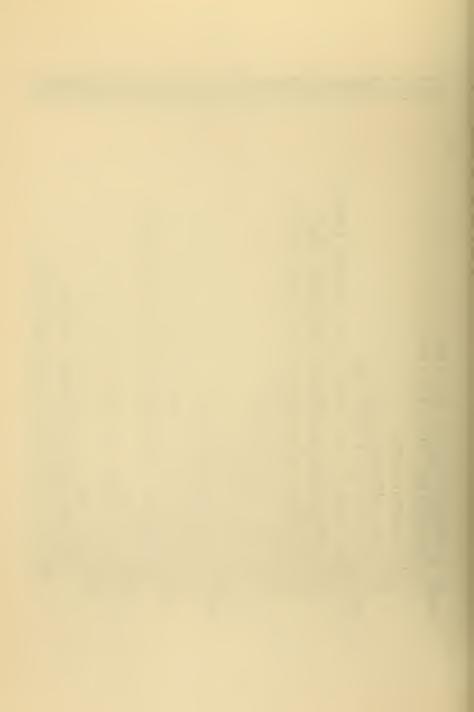
RI = R12; THEN GGTO ENDINST:

FOR R3 := R12; SFF I UNITIL 10 DO

REGIN

RS := R12; RS SECHW:

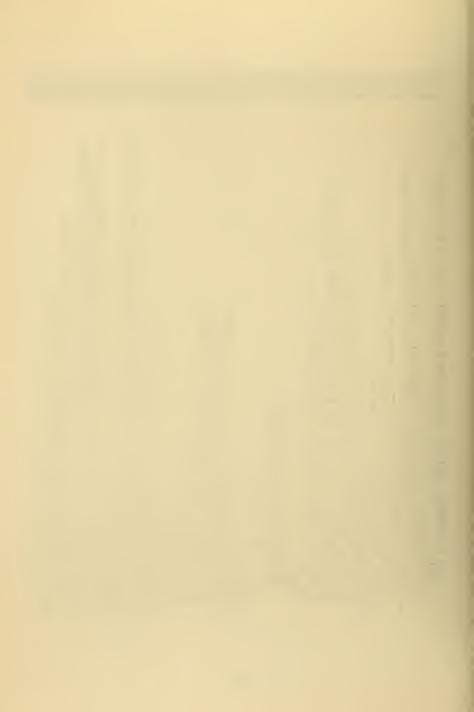
RS := R12; RS SECHW:
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    2
    #0F:
                                                                          R12:
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EGIN
MVC(79,WBUF,CBUF);
MVC(79,WBUF,BLANK)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   32, WBUF," ABOVE
        4 × ··
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R8 := MEMLIMIT; P
S: R0 := aCBUF;
S: THEN GOTO EOIF
IF ECHOI THEN
BEGIN
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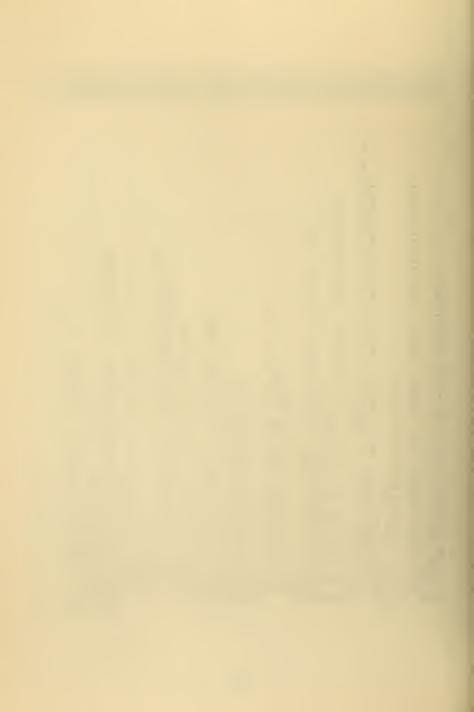
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ADDRESS,
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                                                                                                                                                                                                                                      FORMAT
END: SECHMENTS: ROTO HALF: MYC132, MBUF, BLANK); R1 := 3;

SECHMENTS: FEATURE AND READING INSTRUCTIONS ACCORDING TO ASSEMBLE ASSEMBLE ASSEMBLE ASSEMBLE ASSEMBLE ASSEMBLE ASSEMBLE READING INSTRUCTION FORMAT"); WRITE: MYC127 WBUFF, BLANK READING INSTRUCTION FORMAT"); WRITE: MYC127 WBUFF, BLANK READING INSTRUCTION FORMAT"); WRITE: MYC127 WBUFF, BLANK READING INSTRUCTION FORMAT"); WRITE: RASCHIER READING INSTRUCTION FORMAT"); WRITE: READING INSTRUCTION FORMAT GREATER THAN AND WEFFFFF; WRITE: READING INSTRUCTION FOR STRICT IN THE WRITE: READING INSTRUCTION READING INSTRUCTION READING INSTRUCTION READING INSTRUCTION READING INSTRUMENT IN THE WRITE: WRITE:
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THEN GOTO EOF;
ECHOL THEN
IN
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BLANK)

DESIGNATOR:")

MVC(75,WBUF,B #07 OR #F0; #F0; LATOR DESIGNAT

BUF (37))

M.

STC(R1,

INTEGER SAV14: ARRAY II INTEGER REGWT:

8AV14: BRITE REGWT:

RD := awbuf;

WRITE ROOF ROLLOWENS:

ROUG SAWBUF;

WRITE REGWT:

ROUG SAWBUF;

WRITE RECENT REGIONAL):");

RISE EXECSTATE THEN

ROUG STATE THEN

ROUG STATE THEN

ROUG STATE THEN

ROUG STATE FOR CPU #");

STCRI,WBUF (62);

ROUG STATE FOR CPU #");

STCRI,WBUF (43);

WRITE:

MYC (22,WBUF (43);

WRITE:

MYC (19,WBUF (43);

WRITE:

MYC (19,WBUF (43);

WRITE:

MYC (19,WBUF (43);

WRITE:

ROUG STATUS

R

R1 := LOC; SETZONE(WBUF(30))

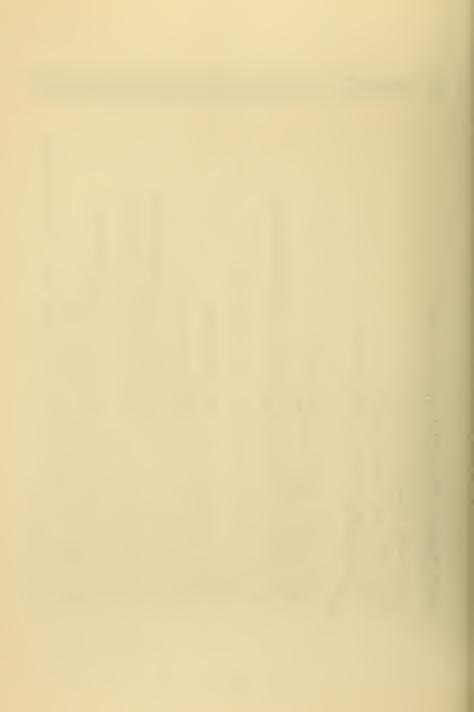
:( "#

17 SHRL

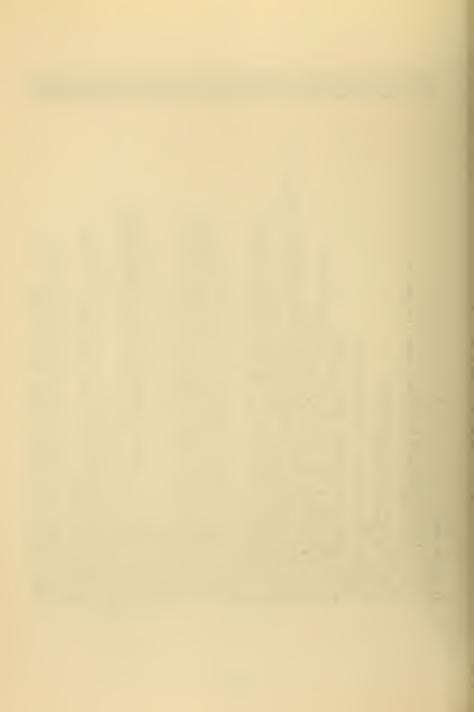
5 # ö #07

AND

90



```
(DECIMAL):")
IAW (IN HEX):");
MVC(50,WBUF,BLANK)
                                    F
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```
SETZONE (WBUF (44))
F2: CMVC(13.WBUF."F2 DESIGNATOR:"); R1 := R6 OR #F0;

STOCK1.WBUF(15);

R1 := 1: R6:= OPERAND: MEX;

R2 := 1: R6:= OPERAND: MEX;

R3 := 1: R6:= OPERAND: MEX;

R4 := 1: R6:= OPERAND: MEX;

R5 := THEN

R6 := THEN

R7 := CMVC(19.WBUF(19.MBVF(3.7.WBUF(3.9).8AVEX);

R7 := CMVC(19.WBUF(19.MBVF(3.7.WBUF(3.9).8AVEX);

R7 := CMVC(19.WBUF(19.MBVF(3.7.WBUF(3.9).8AVEX);

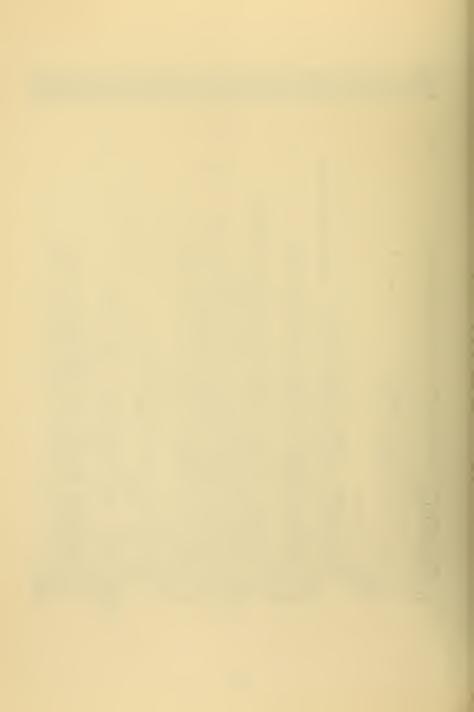
R8 := OPERAND: MEX;

R9 := OPERAND: MEX;

R8 := OPERAND: MEX;

R9 := OPERAND: MEX;

R9 :
```



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DESIGNATOR");
MYC(50, WBUF, "F4 DESIGNATOR: INDEX DESIGNATOR: I DESIGNATOR")

RI := REGWT(16): R2 := R1 SHRL 1 AND #07 OR #F0;

STC(R2, WBUF(36)): R2 := R1 SHRL 1 AND #07 OR #F0;

STC(R2, WBUF(36)): R2 := R1 SHRL 1 AND #07 OR #F0;

STC(R2, WBUF(36)): R2 := R1 SHRL 1 AND #07 OR #F0;

WRITE: MYC(10, WBUF, "ACCUMULATOR A+1 VALUE (IN HEX):"):

BEGIN MYC(30, WBUF, "ACCUMULATOR A+1 VALUE (IN HEX):"):

RX := REGWT(26): "ANEXT: R2 := B2; R1 := 39; WHEX;

MYC(19, WBUF(42): "R1 := 70; WHEX;

END: R1TE: MYC(79, WBUF, BLANK):

FINISH:LM(R3,R13,REGWT): R14 := SAV14:

END:
```



```
BEGIN
INTEGER SAVE14:
PROCEDURE SHIFTAMT (R14); COMMENT OBTAINS THE
BEGIN
```

1458 1459 1460 

```
..
AMOUNT FOR
VALUE IN R6
COMMENT OBTAINS THE SHIFT RUCTIONS 62 - 67 AND RETURNS
                                                    REGSAVESH
                                                                                                                                                                                                                                                                                                              END:
                                                                                                                                    ELD;
                                 BEGIN
SAVI4: ARRAY 3 INTEGER REGSA
SAVI4: STM(R3, R5, REGSAVESH);
R3 := R 4 AND #40;
R5 := R 4 AND #40;
R6 := R 4 AND #40;
R6 := R 4 AND #5;
END ELSE
BEGIN BEGIN BEBIN BEBIN BEBIN BEGIN COMMENT NOOP;
R7 := R 4 AND #20;
R6 := R 4 AND #20;
R7 := R 4 AND #20;
R8 := R 4 AND #20;
R8 := R 4 AND #37;
R8 := R 4 AND #37;
R8 := R 5 AND #37;
END ELSE
BEGIN R8 := I8;
END ELSE
BEGIN R8 := B5 AND #37;
END ELSE
BEGIN R6 := B5 AND #37;
END;
END;
END;
                                                                                                                                                                                                                                                                                                                  u.
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                                                                                                                                                                                                                                                                                                                                                                                                             SA V14;
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ATE ST RUPT # F F F INTERRINTER ADDRESS: TASK STATE; ADDRESS: TASK STATE END : AND R3 ET (EXECSTATE) DORESS: R4 := INST GOTO ENDCASE; SHLL 21; •• ANEXT VV EXECHALF: R4: = R14;

EXECHALF: R4: = INST SHRL 16 ELSE R4

OPCODE = O THEN R4: = INST SHRL 16 ELSE R4

OPCODE = O THEN BEGIN R8: = 15; GOTO E

R7: = ASR AND #F0000; SHRL 5; R6: = ASR SHLL

R83 := ASR AND #F0000; SHRL 5; R6: = ASR SHLL

R84 := ASR AND #F0000; SHRL 5; R6: = ASR SHLL

R85 := ASR AND #F0000; SHRL 5; R6: = ASR SHLL

R85 := ASR AND #F0000; SHRL 5; R6: = ASR SHLL

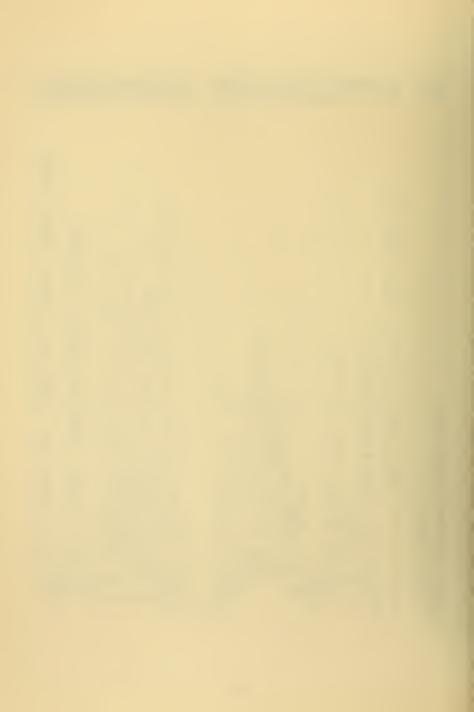
R85 := R84 AND #F0000; SHRL 5; R6: = ASR SHLL

R85 := R84 AND #F0000; SHRL 5; R83 := 4; A

R87 := R84 CPUBASE; COMMENT A(B) ADDRES

R96 IN

R96 IN A ( A ) A ( B )



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61
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                                                                                                                                                                                                                                                                                             DESIGNATOR;
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OPCODE=
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                                                                                                                                                                                                                                   N COMMENT FORMAT IVA INSTRUCTION:
= R4 SHLL 25 SHRL 29; COMMENT SUBFUNCTION CODE I
= R4 AND #21; COMMENT CHECK FOR I DESIGNATOR SET
R3 = 1 THEN SET(IDESIGN) ELSE RESET(IDESIGN);
                                                                                                                           INSTRUCTION
                                                                                                                           IVB
END:

END:

OPCODE > 49 AND OPCODE < 56 THEN

GOTO ADJUSTCPCODE

ELSE

BEGIN

R6 := R4 SHLL 29:

R7 := R4 SHLL 29:

COMMENT SHRL 29:

ADJUSTOPCODE:

OPCODE:

OPCODE:

CASE
OPCODE OF THEN WTRACE:

CASE
OPCODE OF THEN GOTO ILLEGALINST:

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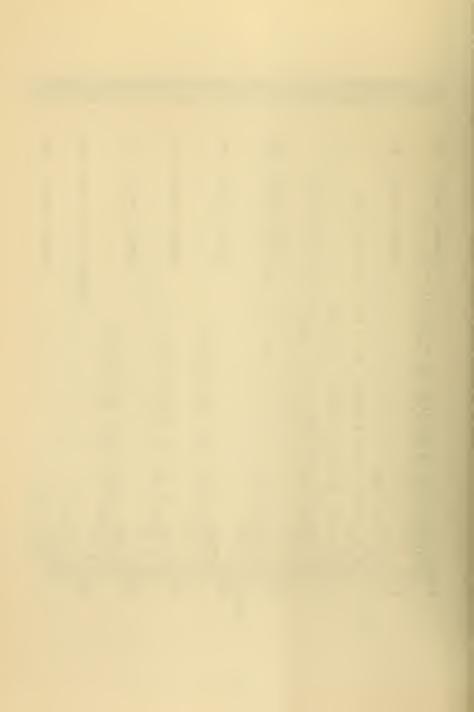
CASE
OPCODE OPCODE

CASE
OPCODE OPCODE

CASE
OPC
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| COMMENT OPCODE = 62;<br>3; R2 := R2 - R2;                                                           | COMMENT OPCODE = 63;                           | B7; R6 := R6 - 32;                                     | B7;<br>R R4; R5 := R5 OR R2;<br>;     | COMMENT OPCODE = 64;<br>R5 - R5; GOTO OP64; END;                                             | COMMENT OPCODE = 65;                                                                                                 | COMMENT OPCODE = 66;                                                                             | COMMENT OPCODE = 67;                                                                                                  | COMMENT OPCODE GROUP 70X;                   | COMMENT OPCODE = 700;       |
|-----------------------------------------------------------------------------------------------------|------------------------------------------------|--------------------------------------------------------|---------------------------------------|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|---------------------------------------------|-----------------------------|
| BEGIN<br>SHIFTAMT: R6 := R6 AND #1F; R3 := B7<br>SLDL(R2,B6); R3 := R3 OR R2; B7 := R:<br>R8 := 18; | END:<br>BEGIN<br>SHIFTAMT:<br>TF R6 >= 32 THEN | BEGIN<br>R3 := B7: R7 := R7 + ANEXT: R5 :=<br>END ELSE | BEGINE BT: RT := RT + ANEXT: R3 := 18 | END:<br>BEGIN<br>SHIFTAMT: IF R6 > 31 THEN BEGIN R5 :=<br>R5 := R7 := R5;<br>OP64: R8 := 18; | END;<br>BEGIN<br>SHIFTAMT:<br>R1 := R7 + ANEXT; R2 := B1; R3 := B7;<br>SRDL(R2,B6); B1 := R2; B7 := R3;<br>R8 := 18; | END:<br>BEGIN<br>SHIFTAMT: IF R6 > 31 THEN R6 := 31;<br>R8 := B7 SHRA R6; B7 := R5;<br>R8 := 18; | END:<br>BEGIN<br>SHITTAMI:<br>RI := R7 + ANEXI: R2 := B1; R3 := B7:<br>SROAFIR2.86): BI := R2; B7 := R3;<br>B8 0 = 18 | END:<br>BEGIN<br>R6:= R6 + 1:<br>CASE R6 OF | BEGIN<br>BEGIN<br>R3 := B7: |



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701:
                                                                                                                                                                        703
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                                                                                                                                                             COMMENT OPCODE
                                                                                                                                                                        COMMENT OPCODE
                                                             COMMENT OPCODE
                                                                                                                                        #80000000#
                                                                                                                  R10:
           OP 7001;
                                                                              THEN GOTO TIME701:
                                                                                                    TIME 701;
                                                                                                                   ŧ
                                                                                                                                        := R2 OR
OP 7012;
                                                                                                                  R10
                                                                                                                             O THEN GOTO OP7011
THEN GOTO OP7011;
                                                                                                                                                                 11;
                             OP 700;
                                                                    œ
           GOTO
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                                                                                                    THEN GOTO
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                                                                                                                                        THEN R2
HEN GOTO
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                             0P7001:
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ANEXT;
THEN
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< 0 AND R10 - 1: TF R
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R22
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R3
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E := 63;
TIME 701;
                                                                                                    IF R7 = R5 OR
OPCODE := 63:
GOTO TIME701:
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                                                                                                                  THEN
                                                                                                              OR
                                                                    II
                                                                                          END:
IF RZ
BEGIN
                                                                                                                                                   OP 7012:
TIME701:
                                                      OP 7001:
                                                                                                                       OP 7011:
                      :00790
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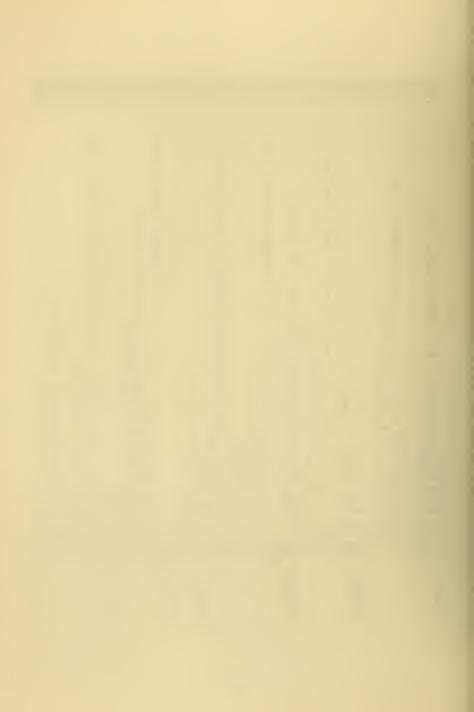


| 0 PC 0 DE = 70 4                                                               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                        |                                     | OPCODE = 711;                      | OPCODE = 712;                     | OPCODE = 713;                        | OPCODE = 714;<br>OPCODE = 715;                | OPCODE = 716;<br>OPCODE = 717;            | CODE = 71X;<br>OPCODE = 72X;<br>OPCODE = 73X;<br>OPCODE = 74X;  | OPCODE = 740;                                | END;<br>- 1; END;                                                                       |                       |
|--------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|--------------------------------------|-----------------------------------------------|-------------------------------------------|-----------------------------------------------------------------|----------------------------------------------|-----------------------------------------------------------------------------------------|-----------------------|
| XOR _1; R8 := R7 + ANEXT; XOR _1; B7 := R2; B8 := R3; R8 := 11; LINST: COMMENT | GALINST: GALINST: COMMENT OGALINST: COMMENT OF COMMENT | בייייייייייייייייייייייייייייייייייייי | : R2 := B7 OR R3; B7 := R2; COMMENT | ; R3 := B5; ADD; B7 := R6; COMMENT | : R3 := B5 XOR _1; ADD; B7 := R6; | : R2 := B7 XOR R3; B7 := R2; COMMENT | ALINST; COMMENT : .R2 := B7 AND R3; B7 := R2; | GALINST: GALINST: COMMENT CASE STATEMENT: | COMMENT END GROUP COMMENT ILLEGAL COMMENT ILLEGAL COMMENT GROUP | COMMENT - D1 - D2 BE. COMMENT                | O THEN BEGIN R2 := R3 XOR 1; R1 := 1;<br>0 THEN BEGIN R2 := R2 XOR 1; R1 := R1<br>* R2; | 0 TH<br>2:= R<br>3 R7 |
| R2 := B<br>N00:<br>11010                                                       | 010<br>010<br>111E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | R6 := R6 + 1<br>CASE R6 OF<br>BFGIN    | EGIN<br>R3 := B5                    | = B7                               | = 87                              | - 85                                 |                                               | END:<br>GOTO ILLE<br>GOTO ILLE            | NN<br>LI<br>VL                                                  | 6 := R6 + 1<br>ASE R6 OF<br>EGIN<br>BEGIN P1 |                                                                                         | R1 == 16 IN R == 17   |



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                          QUOTIENT, R
                                OP741; END;
     COMMENT
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                    RI
                                                                                            GOTO TIME742
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R3 := B7;
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O THEN R7
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                                                                                                       THEN GOTO STORESORT SLDL (R2, 31);
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OR R4 = 1
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Tore
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                                                  R2 := R2 XOR
= R7 - ANEXT;
                                                                                            !!
        = 87
78
!!
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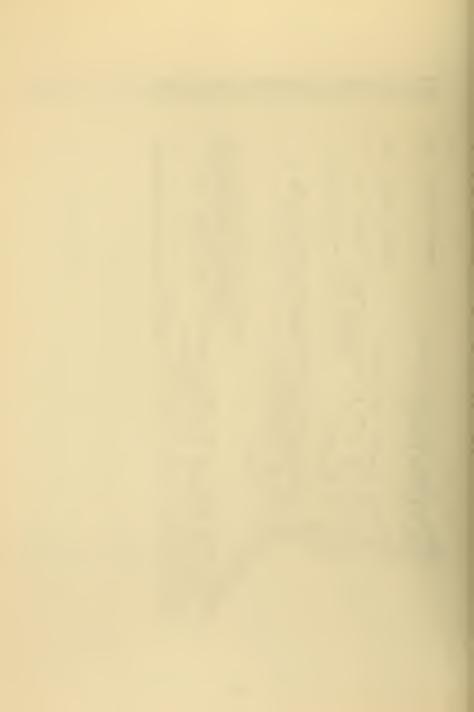




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74X;
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77X;
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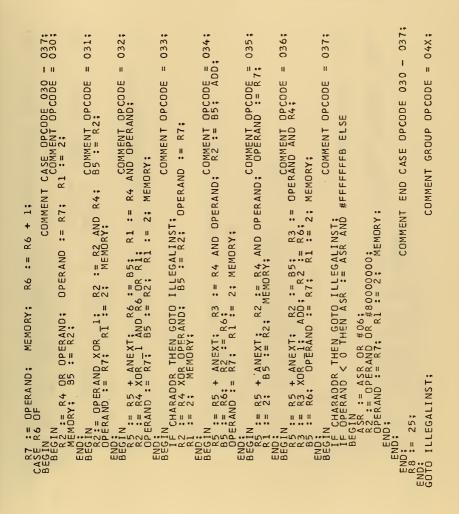


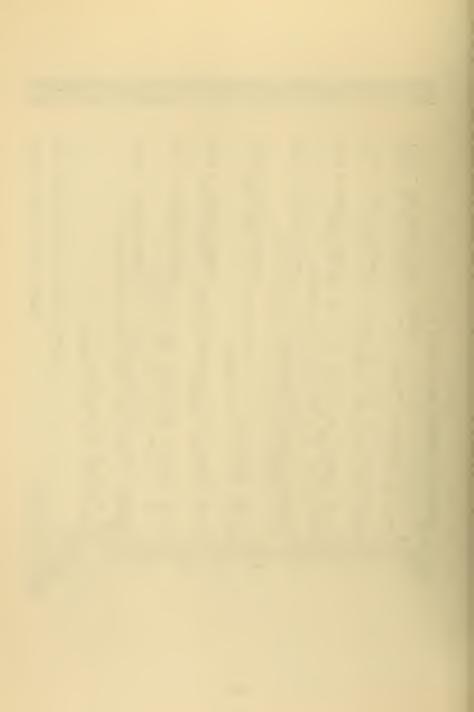
| SEGMENT PROCEDURE FULLWORD (R14);  BEGIN INTEGER SAVE14: SAVE14:= R14: SAVE14:= R14: SAVE14:= R14: CASE OPCODE OF BEGIN MEMORY: R4 := B5; R6 := R6 + R1; CASE R6 OF CASE R6 OF CASE R6 OF CASE R6 OF BEGIN COMMENT CASE OPCODE = 017: BEGIN | OR OPERAND; B5 := R4;  COMMENT OPCODE =  = OPERAND XOR _1; R4 := R4 AND OPERAND; B5:= R4  + ANEXT; R3 := B5; R2 := R4 AND OPERAND;  XOR _1 AND R3 OR R2; B5 := R4; | XOR OPERAND; B5:= R4;<br>+ ANEXT; R2 := B5; R3 :=<br>:= R6; | BEGIN<br>R4 := R4 AND OPERAND; B5 := R4;<br>END;<br>BEGIN<br>R5 := R5 + ANEXT; R2 := B5; R3 := R4 AND OPERAND;<br>R3 := R3 XOR _1; ADD; B5 := R6; | END: BEGIN R5:= R5 + ANEXT: R4 := R4 AND OPERAND; B5 := R4: END: END: R8 := 15; | 86 | AND < |
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| OPERAND := OPERAND SHLL 1;  END; B5 := R3; R8 := 75;  END; ILLEGALINST;  BCTO ILLEGALINST;  BEGIN INST := OPERAND OPCODE = 022;  IF CHARADOR THEN GOTO ILLEGALINST;  R8 := 15; TME: OPERAND: OPCODE := INST SHRL 26;  IF OPCODE = 022;  R8 := 15: TME: OPERAND: OPCODE := INST SHRL 26;  FROCODE = 1NST SHRL 16; ASR := ASR OR #8000;  HALFWORD: R8 := 0; GOTO ENDCASE; | RI := 1: BRANCH; END; BEGIN IF CHARADDR THEN GOTO ILLEGALINST; CHARADDR THEN GOTO ILLEGALINST; MEMORY: INST := OPERAND; OPCODE := INST AND #FC00 SHRL 10; IF OPCODE == 0 THEN HALFWORD; R8 := 15; | END: BEGIN BEGIN R5 := R5 + ANEXT; R3 := B5; R2 := R3 AND R4; R1 := 2; MEMORY; R3 := 15; | END: BEGIN RS := R5 + ANEXT; R2 := B5; R3 := R4; ADD: B5 := R6; R2 := R6; R1 := 2; MEMORY; R8 := 20; | COMMENT OPCODE = | BEGIN<br>IF CHARADDR THEN GOTO ILLEGALINST;<br>R2 := 85; R1 := 2; MEMORY;<br>OPERAND := OPERAND + 1; R5 := R5 + ANEXT; R2 := 85; MEMORY;<br>R8 := 30; | END: END: END: D: GOMMENT GROUP OPCODE - 027; GINEPLACE AND R6 < 7 THEN COMMENT MODIFY STORE ADDRESS FOR INSTRUCTION IN THE REPEAT MODE BY USING \$(6) INSTEAD OF \$(5); ELSE |
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() R4 := B5;

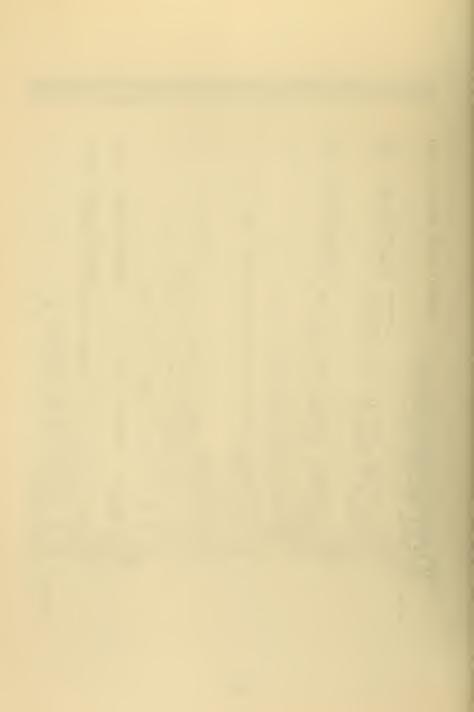
OPERAND THEN R2 := #02;

= OPERAND THEN GOTO EQTEST;

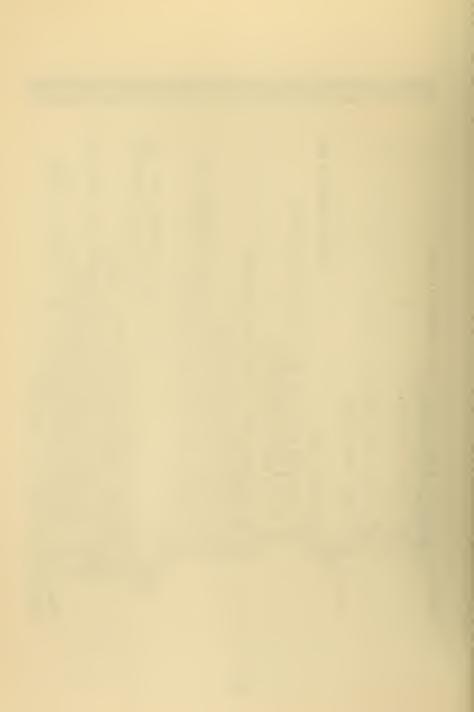
< OPERAND THEN R2 := R2 - R2

- ASR AND #FFFFFFF9 OR R2;

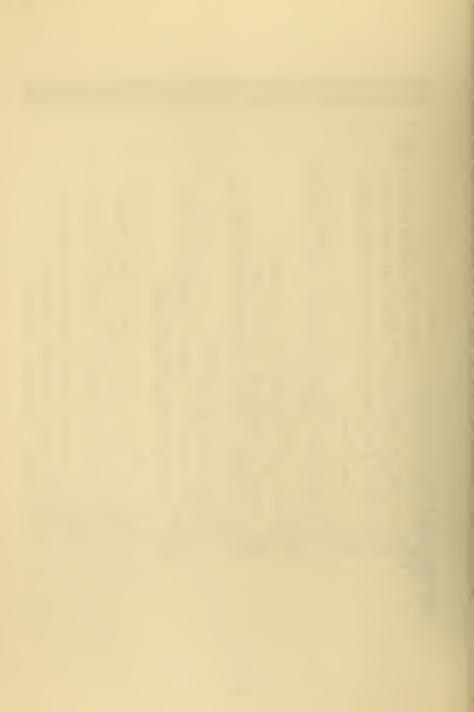
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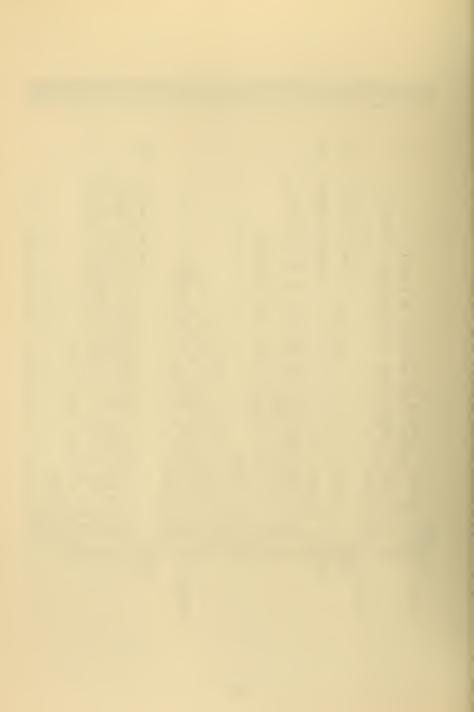
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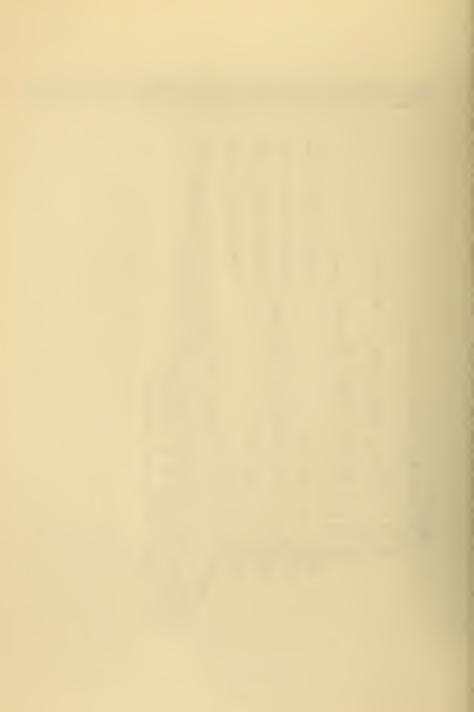
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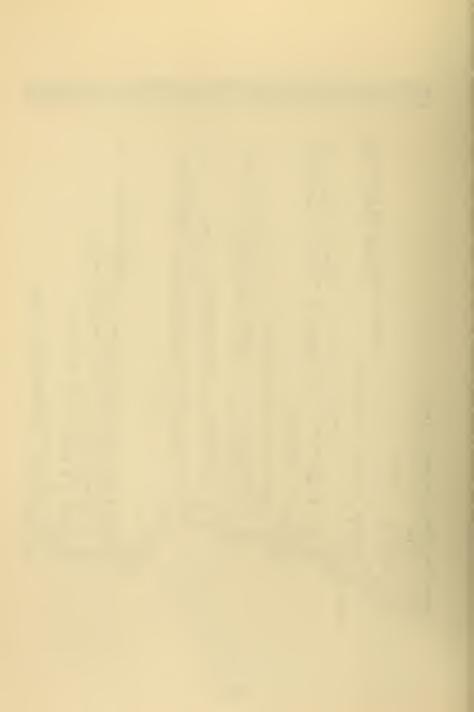
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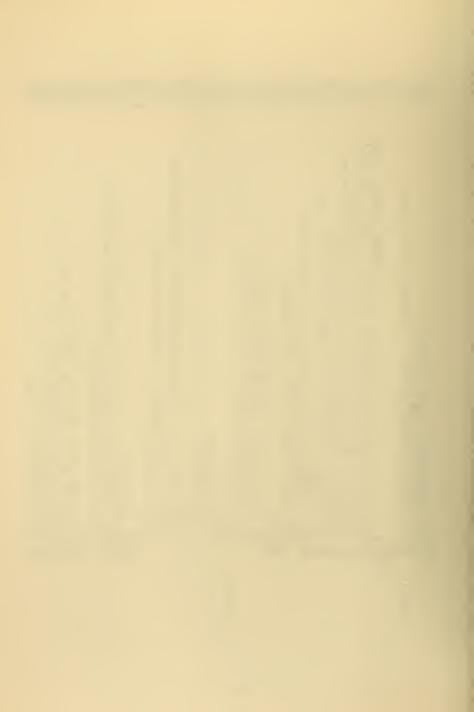
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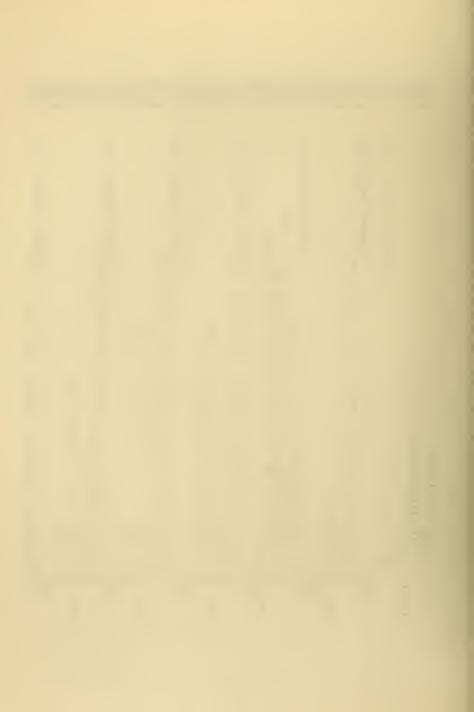
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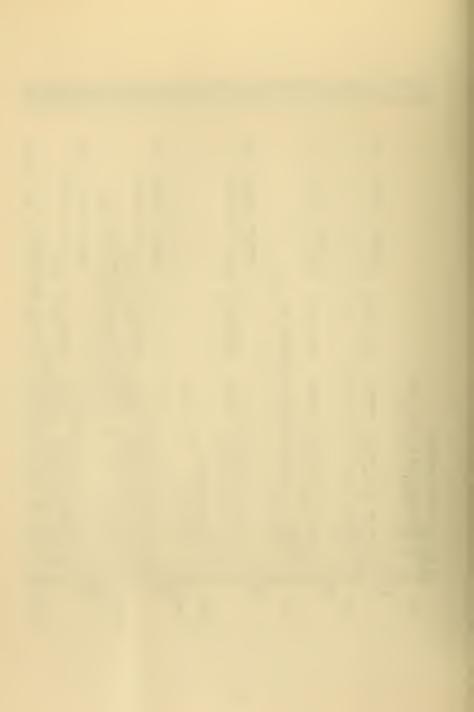
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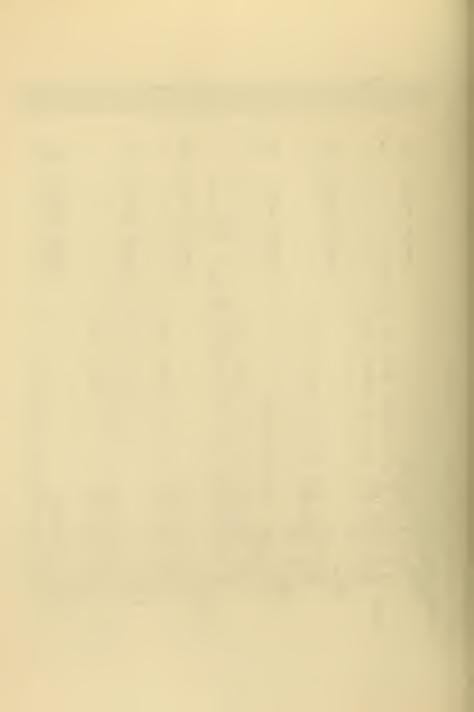
| COMMENT OPCODE = 077;<br>COMMENT OPCODE 10;<br>END;                                                                                                                            | COMMENT OPCODE 11;<br>:= R1; ADO;<br>R6;TATE;                                                                                                                       | COMMENT OPCODE = 12;<br>END;                                                                                                                       | COMMENT OPCODE = 13;<br>END;                                                                               | COMMENT OPCODE = 14;<br>END;                                                                                                     | COMMENT OPCODE = 15;<br>END;                                            |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|
| ELSE (REPEATCMR); RESET(REPEATCMR); RESET(REPEATCMR); END; GOTO ILLEGALINST; END; BEGIN IF CHARADDR THEN BEGIN MEMORY; IF R6 = 0 THEN MEMORY; NORMREAD; CAIO: B5 := 0 GPERAND; | END; BEGIN INDEX THEN GOTO TIMEII; R7 := R6; IF INDEXREGLOC; R2 := B4 AND #FFFF; R3 := R1; R6 := R6 AND #FFFF; R2 := R2 AND #F0000 OR R6; TIME <u>11:</u> R8 := 15; | END: BEGIN  IF CHARADDR THEN BEGIN MEMORY; GOTO CA12; IF R6 = 0 THEN MEMORY; NORMREAD: CA12: R2 := R9 + ANEXT; R8 := R5 + ANEXT; R8 := R5 + ANEXT; | END: BEGIN BEGIN THEN BEGIN MEMORY; GOTO CAI3: IF R6 == 0 THEN MEMORY; NORMREAD: CAI3: R2 := B5; B5 := R6; | END: BEGIN BEGIN IF CHARADDR THEN BEGIN MEMORY; GOTO CA14; IF R6 -= 0 THEN MEMORY; NORMREAD: CA14: R2 := B5; R3 := OPERAND; ADD; | R8 := 15;<br>END;<br>BEGIN<br>IF CHARADDR THEN BEGIN MEMORY; GOTO CAIS; |



|                                                                                                      | GOTO CA16; END; | GOTO CA17; END;<br>ERAND XOR _1;                                                                                                              | COMMENT R5 = B REG ADDRESS;<br>G0T0 CA20; END; |              | COMM<br>= B R<br>END;                                                                                                                                                                                | = K4 AND #FFFF;<br>=FF OR R1; B5 := R6;<br>COMMENT OPCODE = 22;                                      | COMMENT R5 = B REG ADDRESS; GOTO CA22; END; AD; R2 := R2 AND #FFFF; := R6 AND #FFFF OR R1; B5 := R6; |
|------------------------------------------------------------------------------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| IF R6 = 0 THEN MEMORY: NORMREAD: R2 := OPERAND; R3 := B5; ADD: R5 := R5 + ANEXT: B5 := R6; R8 := 15: |                 | END: BEGIN BEGIN IF CHARADDR THEN BEGIN MEMORY; GOTO IF R6 1= 0 THEN MEMORY; NDRME AD: CA17: IF OPERAND < 0 THEN OPERAND := OPERAND R8 := 15: |                                                | CA20: NUMBER | BEGIN<br>BIG R 7 = 0 THE N GOTO TIME21:<br>RS := CPUBASE + INDEXG<br>F CHARADDR THEN BEGIN MEMORY: GOTO CA21:<br>IF CHARADDR THEN BEGIN MEMORY: GOTO CA21:<br>IF R6 = 0 THEN MEMORY: WORMREAD: CA21: | CAZI: RZ := B3; KI := KZ ANU #EUUU; KZ := TMS := DPERAND; ADD; R6 := R6 AND #FIMEZI: R8 := Z0; BEGIN | IF R7 = 0 THEN GOTO TIME22:                                                                          |



| COMMENT OPCODE = 23;                              | AND #FFFF;                |                                                                       | COMMENT OPCODE = 24;                                                           | COMMENT OPCODE = 25; |      | R3 := 1; ADD;<br>OR R6; B5 := R2;                                                                                        | COMMENT OPCODE = 26;                                |                                                                                | COMMENT OPCODE = 27;                                    |                                                                                                          | COMMENT OPCODE = 30;<br>COMMENT OPCODE = 31;                | 25 - 20070                                                            |
|---------------------------------------------------|---------------------------|-----------------------------------------------------------------------|--------------------------------------------------------------------------------|----------------------|------|--------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|--------------------------------------------------------------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|-----------------------------------------------------------------------|
| TIME22: R8 := 20;<br>END;<br>BEGIN - O THEN BECTN | .23; END;<br>XG; R5 := B3 | BEGIN R2 := R5; R1 := 2; MEMORY; END<br>ELSE NORMSTORE;<br>ENR := 15; | BEGIN<br>R5 := B5:<br>R5 CHARADOR THEN<br>BEGIN R2 := R5: R1 := 2; MEMORY; END |                      | ۰۰ ۷ | ELSE NORMSTORE;<br>R5 := INDEXREGLOC; R2 := B5 AND #FFFF;<br>R6 := R6 AND #FFF; R2 := R2 AND #F0000<br>TIME25: R8 := 15; | END:<br>8EGIN<br>RS := 85 XOR I;<br>15 := 85 XOR I: | BEGIN R2:= R5; R1 := 2; MEMORY; END ELSE NORMSTORE; R1 := 15; MEMORY; END END: | BEGIN<br>R5 := B5:<br>IF R5 < 0.0 THEN R5 := R5 XOR _1: | IF CHARADUR I I I I I I MEMORY; END BEGIN R2:= 15; MEMORY; END ENS I I I I I I I I I I I I I I I I I I I | GOTO ILLEGALINST;<br>GOTO ILLEGALINST;<br>GOTO ILLEGALINST; | DEGIN CHARADDR THEN GOTO ILLEGALINST;<br>IF R7 > 12 THEN GOTO TIME32; |





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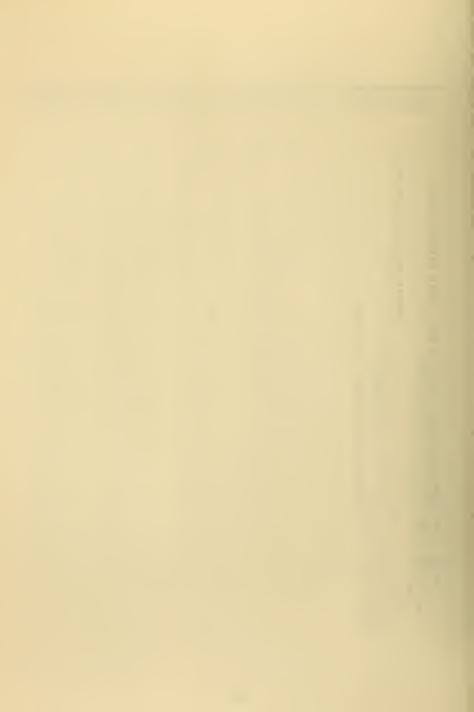
COMMENT R6 INDICATES NEGATIVE REMAIN
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         CA40:
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STATEMENT
       END:
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     GOTO TIME 47;
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   BEGIN ASR := ASR OR #06;
ASR := ASR OR #02;
IF R6 > R5 THEN BEGIN ASR := ASR OR #02;

TIME47: R8 := 15;
END:
END CASE: TIME: MEM (CPUBASE + 100) := ASR;
ILLEGALINST:R1 := 2; R2 := R1; INTERRUPT;
FINISH:R14 := SAVE14;
END:
COMMENT END PROCEDURE FULL
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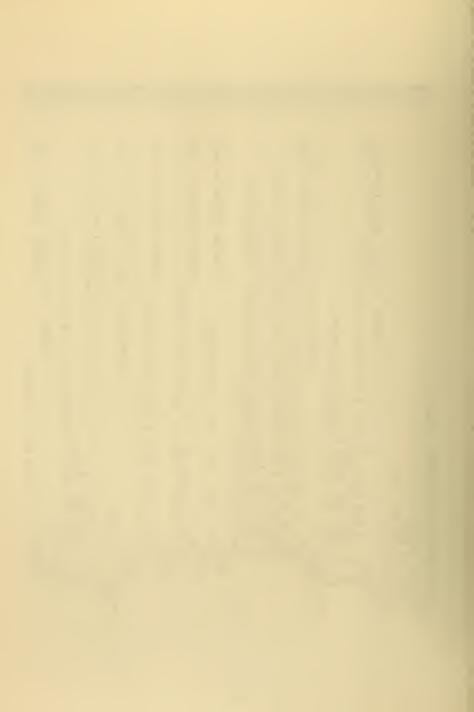
RAFEGE SAVE14:
CASE OPCODE OF
BEGIN

RAF := R6 SARD

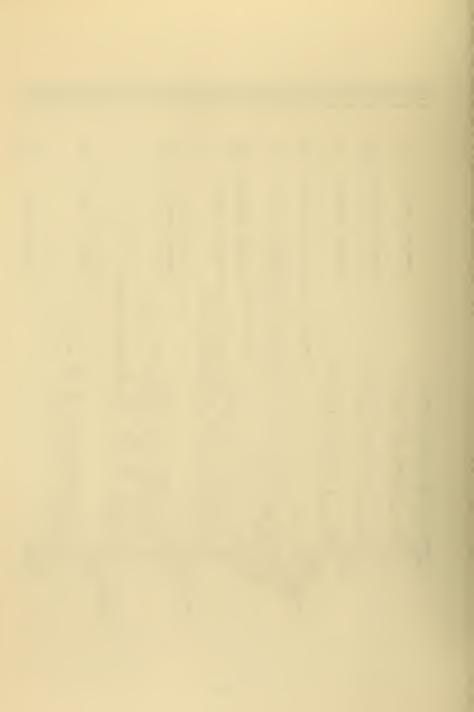
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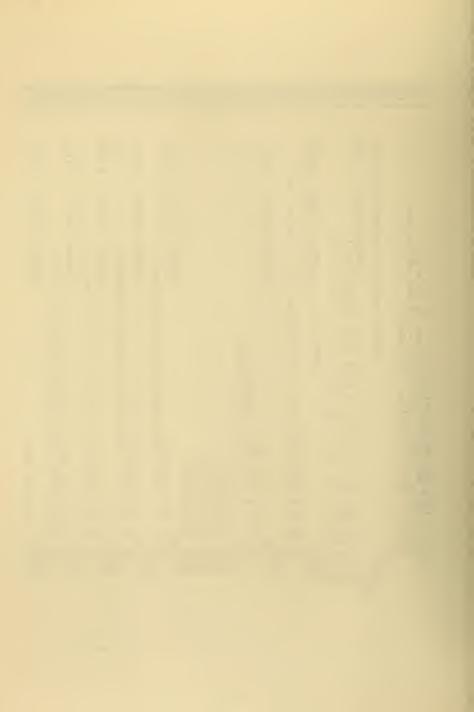
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| COMMENT OPCODE = 511;<br>COMMENT OPCODE = 512;                                                                                | COMMENT OPCODE = 513;                                                                                                 | COMMENT OPCODE = 52X;<br>COMMENT CASE OPCODE OF 529 - 523; | COMMENT OPCODE = 5 AEM(CPUBASE + 328); 4; ( R4; | COMMENT OPCODE = 521;<br>= 85;<br>. OR R4;                                                                                                                                                                                                                                                     | COMMENT OPCODE = 522;                                                                                                                                 | COMMENT OPCODE = 523; |
|-------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| MEM(CPUBASE + 328) := R7; END; BEGIN IFRS > 0 THEN GOTO TIME51X; END; BEGIN ENCPUBASE + 328) := R7; AEM(CPUBASE + 328) := R7; | END;<br>BEGIN<br>1 FRS = 0 THEN GOTO TIME51X;<br>MEM(CPUBASE + 328) := R7;<br>END;<br>END;<br>END;<br>END;<br>COMMENT | H                                                          | 77.77<br>77.77<br>#E0<br>DEXR                   | BEGIN<br>BEGIN<br>IF R 7 = 0 THEN GOTO TIME521;<br>R5 := CPJBASE + INDEXE + R7; R4 := E<br>IF K 4 = 0 THEN GOTO TIME521;<br>R4 := R4 - R1; B5 := R4;<br>R4 := INST AND #E000 SHUL 4;<br>R7 := INST AND #EFOR SHUL 4;<br>R7 := INST AND #EFOR SHUL 4;<br>R7 := INST AND #FIFFF + INDEXREGVAL OF | TIME521: R8 := 18:  END:  BEGIN  R3 := INDEXREGLOC; R3 := B3;  R4 := INST AND #FFFF + R3 AND #FFFF;  R2 := R3 AND #E0000 OR R4;  R8 := L5:  R8 := L5: | END:<br>BEGIN         |



| R4 := INST AND #E000 SHLL 4; R7 := INST AND #IFFF + INDEXREGVAL OR R4 + R1; R7 := INST AND #IFFF + INDEXREGVAL OR R4 + R1; R8 = 15; R8 := 15; COMMENT END CASE OPCODE = 52X | AND #01: IF R3 > 0 THEN GOTO ILLEGALINST: SHRL 1: IF R5 >= 2 THEN GOTO 0P532; OF SHRL 2: R6 := R6 SHRL 1 SHLL 3 OR R7 + R1; OF COMMENT CASE OPCODE OF 5300 - 53 | R4 := ASK AND #08;  R5 | LLEGALINST;<br>LLEGALINST;<br>LLEGALINST;<br>LLEGALINST;<br>LLEGALINST;<br>LLEGALINST; | BEGIN<br>R4 := ASR AND #04;<br>IF R4 > 0 THEN GOTO TIME53X ELSE GOTO SETBR53;<br>FND: | BEGIN<br>R4 := ASR AND #04;<br>IF R4 = 0 THEN GOTO TIME53X ELSE GOTO SETBR53;<br>FND: | BEGIN<br>R4 := ASR AND #06:<br>IF R4 = 2 THEN GOTO SETBR53 ELSE GOTO TIME53X;<br>FND: | BEGIN<br>R4 := ASR AND #02:<br>IF R4 > 0 THEN GOTO SETBR53 ELSE GOTO TIME53X; | BEGIN<br>COMMENT OPCODE = 5314;<br>R4 := ASR AND #02; |
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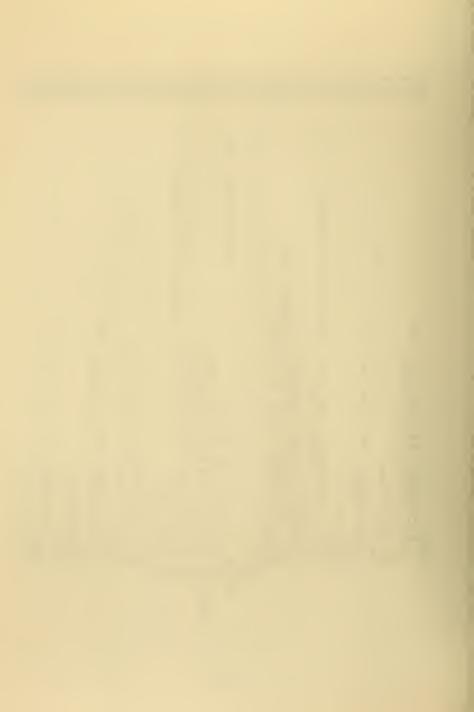


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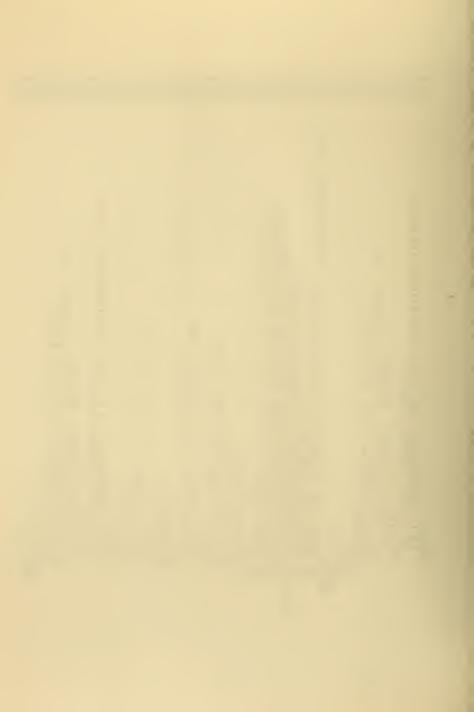


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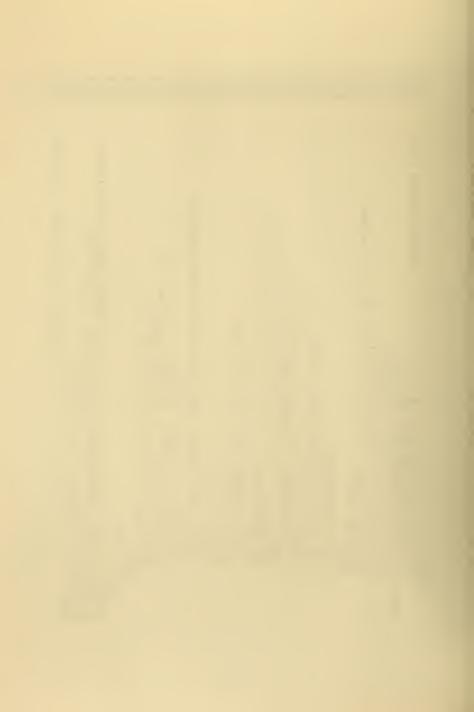
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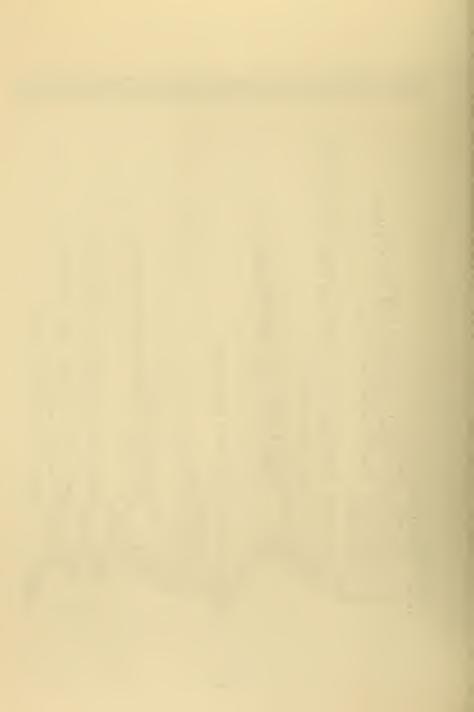
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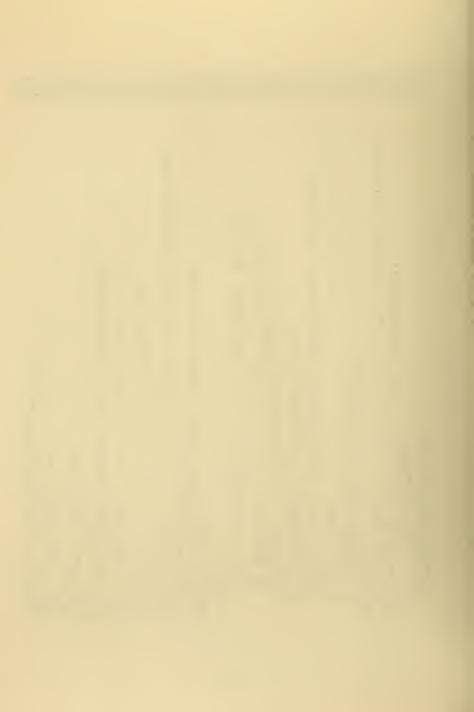
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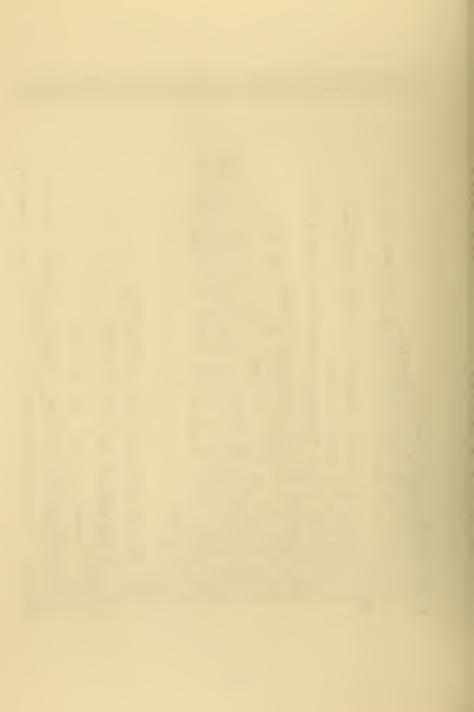
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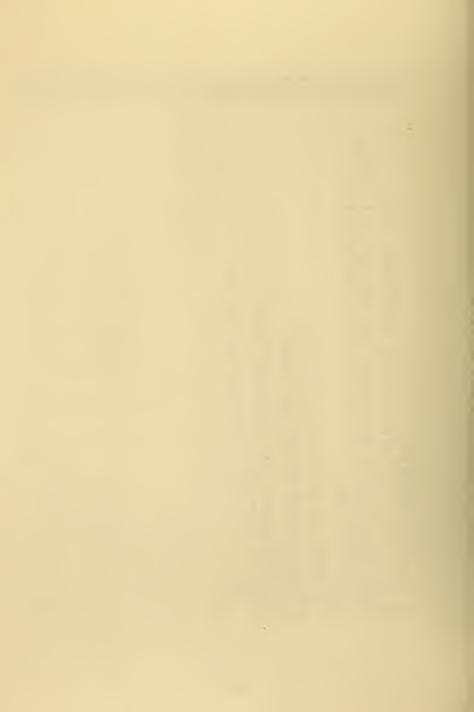
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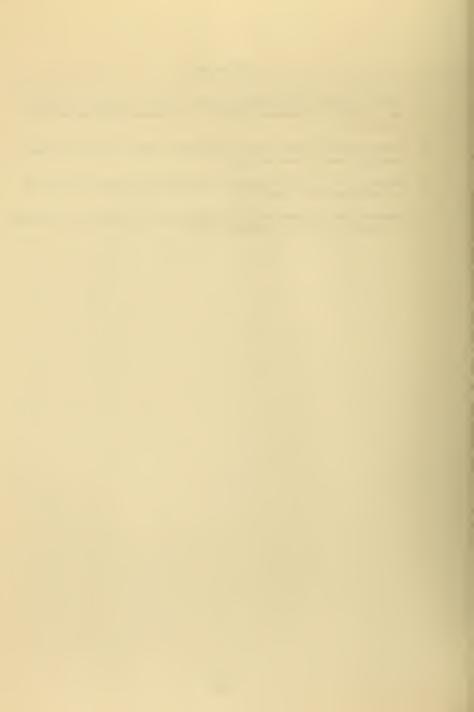


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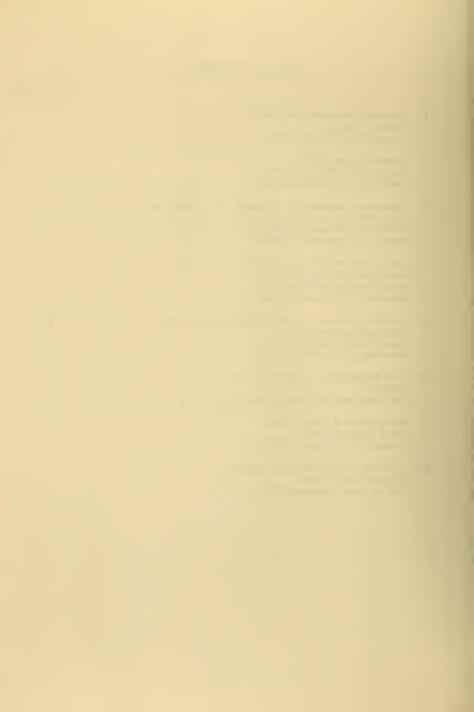
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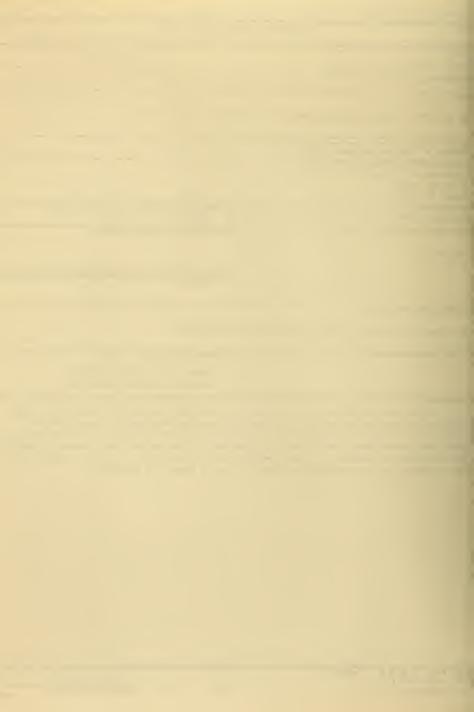
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| AN AN/UYK-7 Interpreter Implemented On The IBM System/360                                                                                                         |                                                                |              |                 |  |  |  |
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| Allen B. Webb                                                                                                                                                     |                                                                |              |                 |  |  |  |
| James R. King                                                                                                                                                     |                                                                |              |                 |  |  |  |
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| 13. ABSTRACT                                                                                                                                                      |                                                                |              |                 |  |  |  |
| An IBM System/360 based interpreter program for the AN/UYK-7 multiprocessing                                                                                      |                                                                |              |                 |  |  |  |
| In the byttem, the transfer interpretive execution of                                                                                                             |                                                                |              |                 |  |  |  |

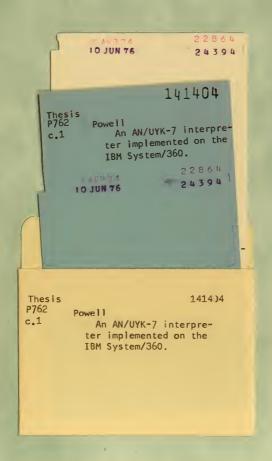
An IBM System/360 based interpreter program for the AN/UYK-7 multiprocessing computer system is presented. The program provides interpretive execution of the AN/UYK-7 instruction set, an interrupt-handling capability, a variable-sized simulated memory and a multiprocessing capability for up to three central processors. Unput/output is limited to a card reader and a line printer. Various segments of the program are discussed and a detailed User's Manual is provided.



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